Module 5

DC to AC Converters

Lesson 37

Sine PWM and its Realization

After completion of this lesson, the reader shall be able to:

1. Explain the concept of sine-modulated PWM inverter
2. Design a simple controller for the sine-PWM inverter
3. Calculate output voltage magnitude from the inverter operating parameters
4. Compare sine-modulated PWM inverter with square wave inverter

The PWM inverter has been introduced in Lesson 36 and Fig. 36.1 shows a typical pole voltage waveform, over one output cycle of the PWM inverter. It can be seen that the pole voltage consists of large number of rectangular pulses whose widths are modulated suitably to provide control over the output voltage (fundamental component) magnitude and, additionally, control over the harmonic spectrum of the output waveform.

In Sine-PWM inverter the widths of the pole-voltage pulses, over the output cycle, vary in a sinusoidal manner. The scheme, in its simplified form, involves comparison of a high frequency triangular carrier voltage with a sinusoidal modulating signal that represents the desired fundamental component of the pole voltage waveform. The peak magnitude of the modulating signal should remain limited to the peak magnitude of the carrier signal. The comparator output is then used to control the high side and low side switches of the particular pole. Fig. 37.1 shows an op-amp based comparator output along with representative sinusoidal and triangular signals as inputs. In the comparator shown in Fig. 37.1, the triangular and sinusoidal signals are fed to the inverting and the non-inverting input terminals respectively and the comparator output magnitudes for high and low levels are assumed to be $+V_{CC}$ and $-V_{CC}$.

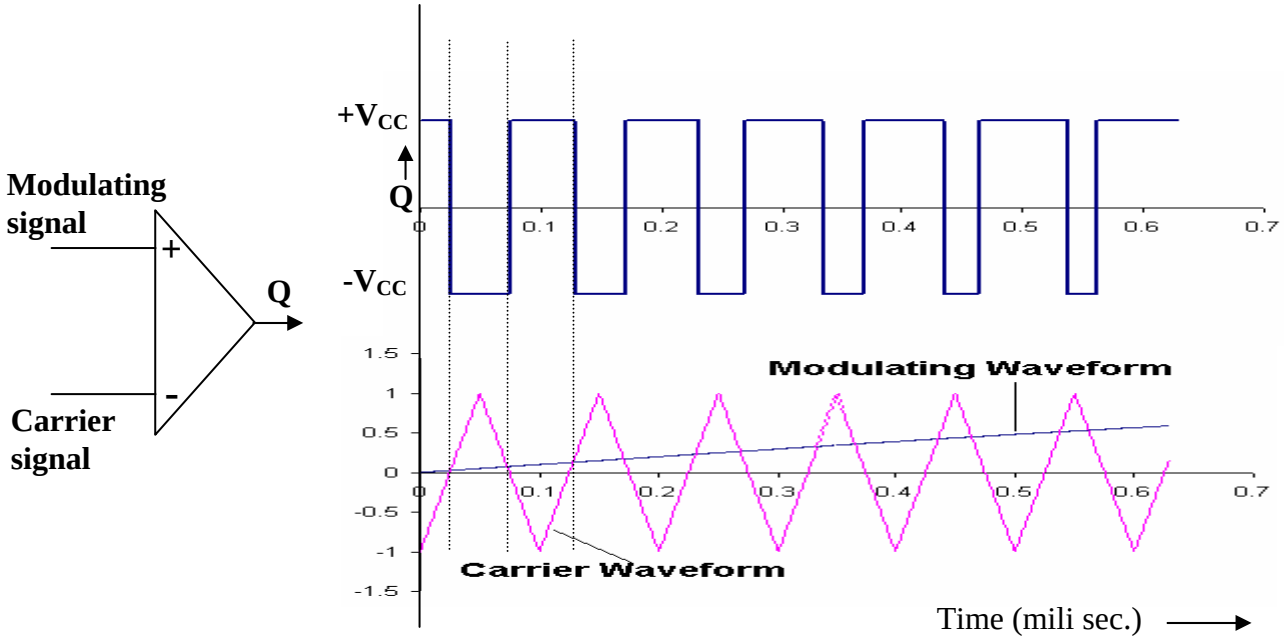

Fig. 37.1: A schematic circuit for comparison of Modulating and Carrier signals

The comparator output signal 'Q' is used to turn-on the high side and low side switches of the inverter pole. When 'Q' is high, upper (high side) switch of the particular pole is turned on and when 'Q' is low the lower switch is turned on.

The pole voltage, thus obtained is a replica of the comparator output voltage. When 'Q'= + V_{CC}, the pole voltage (measured with respect to the mid potential point of the dc supply) is $+0.5E_{dc}$ and

when 'Q'= (-)V_{CC}, the pole voltage becomes (-0.5)E_{dc}. The input dc voltage to the inverter (E_{dc}) has been assumed to be of constant magnitude. Thus, on a normalized scale, the harmonic contents in the comparator output voltage and the pole voltage waveforms are identical.

37.1 Analysis Of The Pole Voltage Waveform With A Dc Modulating Signal

Before analyzing the sine-modulated pole voltage waveform, it would be revealing to consider a pure dc signal (of constant magnitude) as the modulating wave. The magnitude of the dc modulating signal is constrained to remain between the minimum and maximum magnitudes of the triangular carrier signal. Fig. 37.2 illustrates one such case where the triangular carrier signal varies between -1.0 and +1.0 units of voltage and the magnitude of the modulating wave is kept at 0.4 unit of voltage. Now, the high frequency triangular carrier waveform is compared with the dc modulating signal and the comparator output is used to control the high and low level switches (S_U and S_L respectively) of the inverter pole shown in Fig. 37.2.

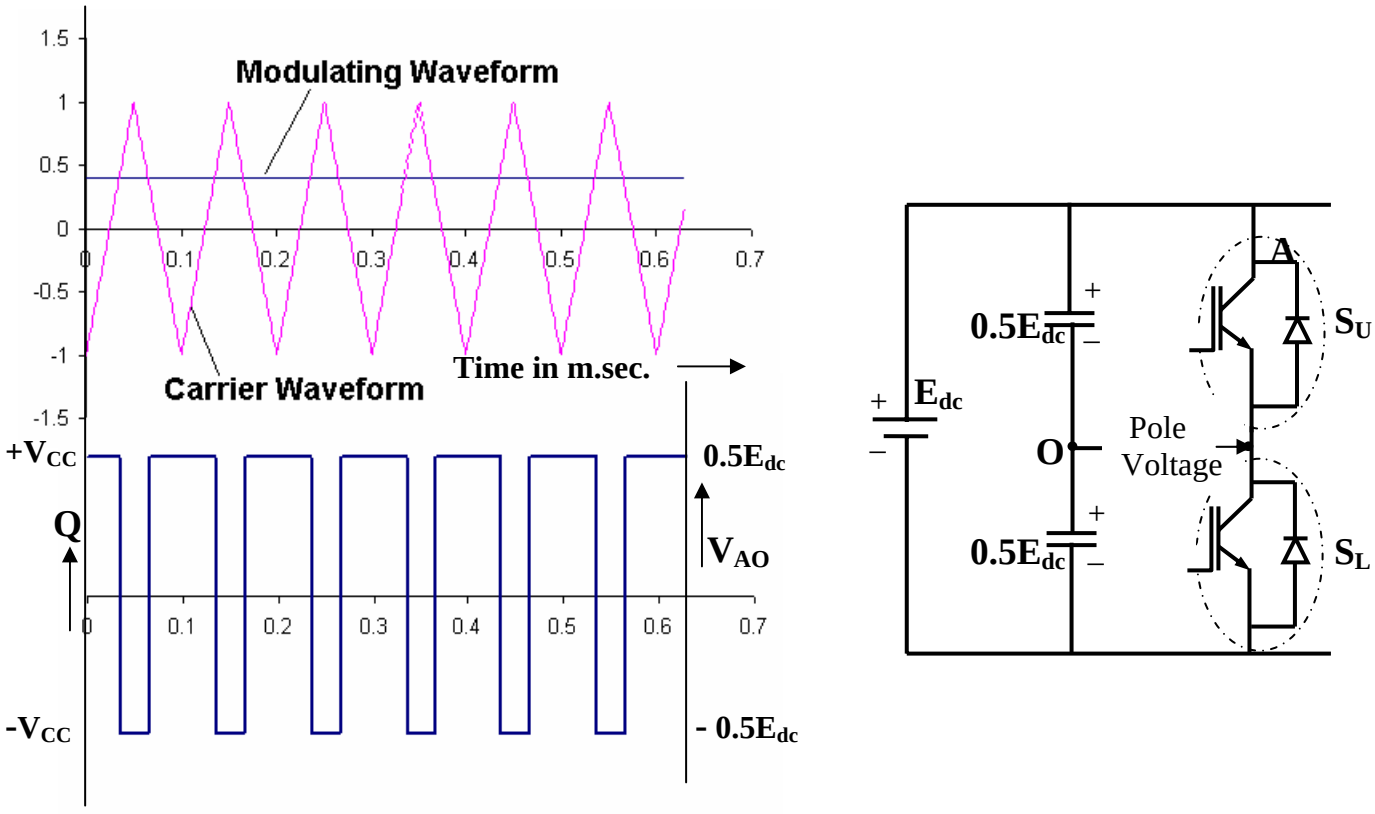

Fig. 37.2: Inverter pole voltage for a pure dc modulating waveform

The figure also shows the comparator output (Q) and the pole voltage (V_{AO}) waveforms for this case. As can be seen, with pure dc modulating signal the pole voltage consists of pulses of identical shapes repeating at carrier frequency. The Fourier series decomposition of pole voltage waveform results into a mean (dc) voltage and harmonic voltages whose frequencies are integral multiples of carrier frequency. By using simple mathematics the high-duration of the pulses (t_h), during which the pole voltage magnitude is $0.5E_{dc}$, can be found to be

$$t_h = \frac{T_c}{2}(1+\frac{V_m}{\widehat{V_c}}) \text{ ..... (37.1),}$$

where T_c is the time period of the triangular carrier waveform, V_m is the magnitude of the modulating signal and $\widehat{V_c}$ is the peak (positive) magnitude of the carrier signal.

In a similar manner the low-duration (t_l) of pulses during which the pole voltage magnitude is -0.5E_{dc}, can be found as:

$$t_l = \frac{T_c}{2}(1-\frac{V_m}{\widehat{V_c}}) \text{ ..... (37.2)}$$

The dc component of the pole voltage (V_0) can be found to be

$$V_0 = 0.5E_{dc}\frac{V_m}{\widehat{V_c}} \text{ ..... (37.3)}$$

The dc modulating signal could acquire any magnitude between $+\widehat{V_c}$ and $-\widehat{V_c}$ and accordingly the mean magnitude of pole voltage can vary within +0.5E_{dc} and -0.5E_{dc}. When the modulating signal magnitude (V_m) is zero, the high and low durations of the pole output pulses will be identical and the mean pole voltage magnitude will be zero.

As mentioned before, apart from the dc component, the pole voltage consists of harmonics of integral multiples of carrier frequency. The lowest order harmonic-frequency being same as the carrier frequency.

37.2 Pole Voltage Waveform With Sinusoidal Modulating Signal

In the previous section a pure dc modulating signal was considered. Let now a slowly varying sinusoidal voltage, with the following constraints, be considered as the modulating signal:

1. The peak magnitude of the sinusoidal signal is less than or equal to the peak magnitude of the carrier signal. This ensures that the instantaneous magnitude of the modulating signal never exceeds the peak magnitude of the carrier signal.
2. The frequency of the modulating signal is several orders lower than the frequency of the carrier signal. A typical figure will be 50 Hz for the modulating signal and 20 Kilohertz for the carrier signal. Under such high frequency ratios, the magnitude of modulating signal will be virtually constant over any particular carrier-signal time period.

Because of the above assumptions some results of the previous section, where a pure dc modulating signal was considered, may be used. Since the slowly varying modulating signal is virtually constant over a high frequency carrier time period, the mean magnitude of the inverter pole voltage averaged over a carrier time period will be proportional to the mean magnitude of the modulating signal. Thus the discretely averaged magnitude of pole voltage (averaged over successive high frequency carrier time period) is similar to the modulating signal. The pole voltage waveform thus has a low frequency component whose instantaneous magnitude is

proportional to the modulating signal (also implying that they will have same frequency and will be in-phase). Apart from this low frequency component the pole voltage will also have high frequency harmonic voltages. However, unlike in the case of pure dc modulating signal the harmonic frequencies are now not simply integral multiples of carrier frequency. This is so because here the widths of the high frequency pole-voltage pulses do not remain constant through out. The pulse widths get modulated as per equations (37.1) and (37.2) due to slowly varying modulating signal. As a result the harmonics in the pole voltage waveform are of frequencies that are shifted from the carrier (and multiples of carrier frequency) by the integral multiples of modulating wave frequency. In fact one gets a band of harmonic frequencies centered around the carrier and integral multiples of carrier frequency. The individual frequencies that form the band are displaced from these central frequencies by integral multiples of modulating wave frequency. However, the modulating wave frequency being negligible compared to the carrier frequency, the dominant harmonics are still in the vicinity of carrier frequency and multiples of carrier frequency. A more detailed harmonic analysis of the sine-modulated pole voltage waveforms is beyond the scope of this course. The low frequency (modulating frequency) component of the pole output voltage is often referred as fundamental frequency component.

Now, in some cases the ratio of carrier and modulating frequencies may not be very high but the pole voltage still has a fundamental frequency component proportional to and in-phase with the modulating signal. The essential advantage of having very high carrier frequency, in comparison to the modulating wave frequency, is that the useful fundamental frequency component of pole voltage and the unwanted harmonics (having frequencies close to the carrier and multiples of carrier frequency) are far apart on the frequency spectrum and one can virtually filter away the harmonic voltages without attenuating the magnitude of the fundamental frequency component by putting a suitable low pass filter. The filter size requirement remains small if the harmonics are of high frequencies. In some applications, like ac motor drive application, the inherent low pass filtering characteristics of the motor-load itself is enough to satisfactorily block the flow of harmonic currents to the load. In such cases the need for external filter may not arise.

It may be obvious that high carrier frequency calls for high switching frequency of the inverter switches. In fact the switches turn-on and turn-off once during each carrier cycle. Generally the switches used in high power applications (say, more than few hundred kW) can be switched only at sub kilohertz frequency and hence the carrier frequency cannot be arbitrarily high. The switching frequency related losses are also to be considered before deciding the carrier frequency of the sine-PWM inverter.

What Is Modulation Index?

Modulation index is the ratio of peak magnitudes of the modulating waveform and the carrier waveform. It relates the inverter's dc-link voltage and the magnitude of pole voltage (fundamental component) output by the inverter. Now let '$\widehat{V_m}\sin(\omega t)$' be the modulating signal and let the magnitude of triangular carrier signal vary between the peak magnitudes of $+\widehat{V_c}$ and $-\widehat{V_c}$. The ratio of the peak magnitudes of modulating wave ($\widehat{V_m}$) and the carrier wave ($\widehat{V_c}$) is defined as modulation-index (m). In other words:

$$m = \frac{\widehat{V_m}}{\widehat{V_c}} \quad \text{……... …...(37.4)}$$

Normally the magnitude of modulation index is limited below one (i.e., $0 < m < 1$). From the discussion in the previous section it can be concluded that for $0 < m < 1$, the instantaneous magnitude of fundamental pole voltage ($V_{AO,1}$) will be given by:

$$V_{AO,1} = 0.5E_{dc}(m \sin \omega t) \quad \text{……... …...(37.5),}$$

where 'ω' is the angular frequency of the modulating waveform. For $m = 1$ the pole output voltage (fundamental component) will have a rms magnitude of $0.35E_{dc}$ ($= \frac{1}{2\sqrt{2}} E_{dc}$). This magnitude, as can be found out from Sec. 34.1 of Lesson 34, is only 78.5% of the fundamental pole voltage magnitude output by a square wave inverter operating from the same dc link voltage.

What Is Over-Modulation?

When the peak magnitude of modulating signal exceeds the peak magnitude of carrier signal (resulting in $m > 1$), the PWM inverter operates under over-modulation. During over-modulation the fundamental component of the pole voltage increases slightly with increase in modulation index but the linear relation between them, as shown by Eqn. (37.5), no longer continues. Also, lower frequency harmonics crop up in the pole-output waveform. It may easily be seen that for 'm' very high (say m = infinity), the pole voltage shape will be identical to the square wave shape discussed in Lesson-34. Over modulation is generally not preferred because of the introduction of lower frequency harmonics in the output waveform and subsequent distortion of the load current.

37.3 A 1-Phase Sine-PWM Inverter Of H-Bridge Topology

Lesson-34 shows the half bridge and full bridge topologies of a single phase square-wave inverter. The single-phase full bridge is also called as H-bridge because of its resemblance with the letter 'H'. [The two legs (poles) of the inverter resemble the two vertical lines of 'H' and the horizontal line denotes the load, which is connected to the pole output points.] The switches and the load in a single-phase full bridge PWM inverter are connected exactly as in a square-wave inverter circuit. The difference lies in the conduction pattern of the inverter switches. In the square-wave inverter the switches conduct continuously for 180^0 in each output cycle whereas in PWM inverter large number of switching take place in each output cycle.

The half bridge sine-PWM inverter employing only one leg has already been described in the previous section. The full bridge inverter employs one additional leg but the control signals of the half bridge circuit may still be employed for switches of the other leg. As in the square-wave inverter (Lesson-34) the diagonal switches of the two legs may be turned on together to produce a load voltage that has double the magnitude of individual pole voltage. The PWM signals for the high and low level switches of one leg (obtained by sine-triangle comparison) may again be used for low and high level switches, respectively, of the other leg.

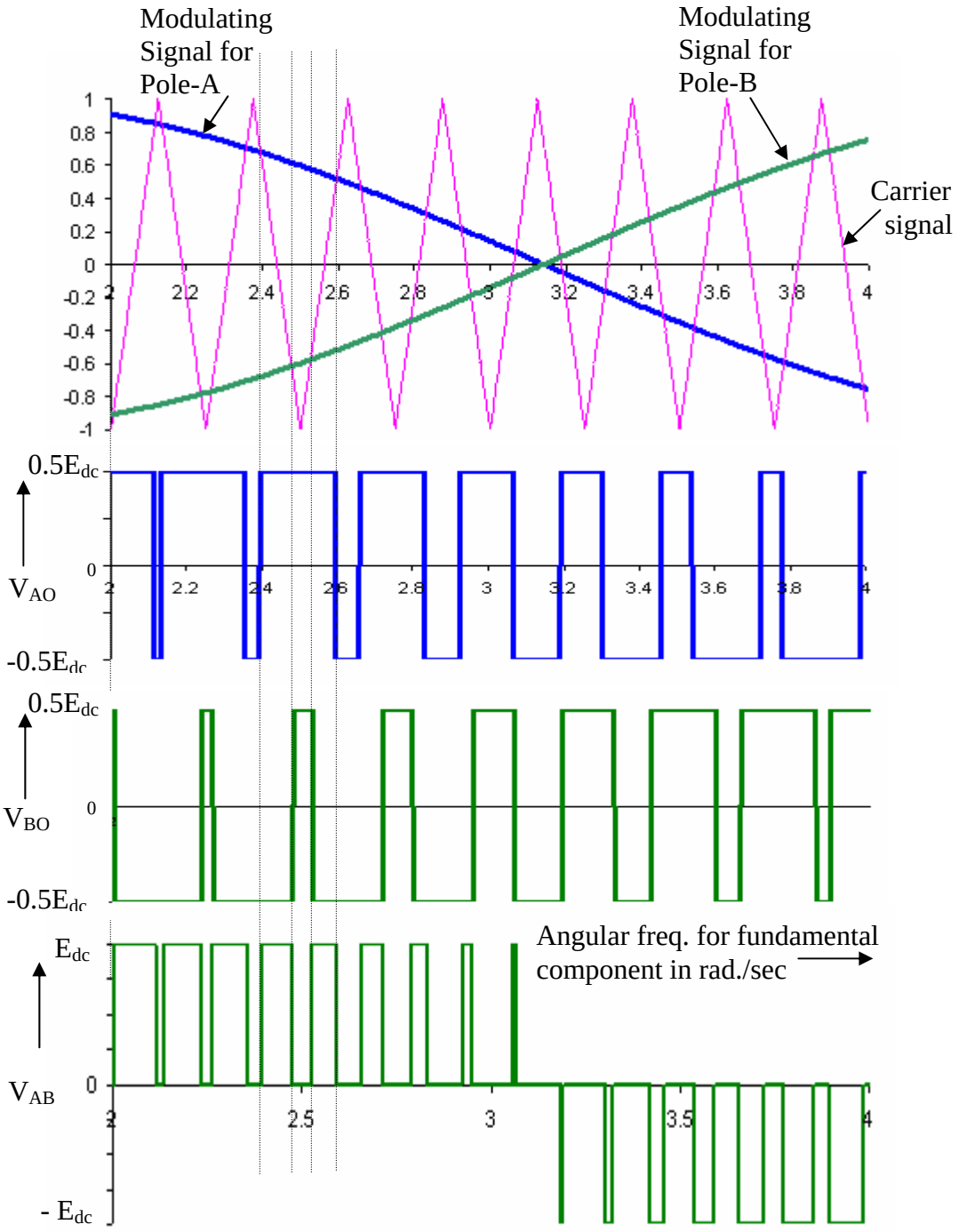

Fig. 37.3: Sine-PWM waveforms for single-phase H-Bridge inverter

Alternately (also, preferably), the modulating waveform for the other leg may be inverted (keeping the carrier waveform same). The two inverted modulating waveforms are then compared with the same carrier waveform using two different comparators. The comparator outputs, one for each leg, are then used to switch the high and low level switches as in the half bridge circuit.

Fig.37.3 shows the relevant waveforms that use two inverted sine waves as modulating signals for the two legs of the inverter. For better visibility the ratio between the carrier and modulating

wave frequencies has been assumed equal to 'eight' (normally carrier frequency is much higher) and circuit waveforms for only part of the modulating wave cycle has been shown. In Fig.37.3, the blue colored modulating wave is used for pole-A of the inverter and the green colored for pole-B. The corresponding pole voltages (V_{AO}, V_{BO}) and the load voltage (V_{AB}) are also shown in the figure.

The scheme, using two inverted modulating waves, has the following advantages over the one that uses single modulating wave and employs simultaneous switching of the diagonal switches of the two legs:- (i) Overall harmonic distortion of the load voltage waveform is reduced and (ii) the frequency of the ripple voltage in the load waveform doubles. Both these points may be verified by mere inspection of the load voltage waveform shown in Fig.37.3. In case of single modulating wave, the instantaneous load voltage has double the amplitude of pole-A voltage and thus the harmonic distortion of the load voltage and pole voltage remains same. It may be noted that the instantaneous magnitude of load voltage, in this case, has two levels ($+0.5E_{dc}$ and $-0.5E_{dc}$). In the alternate scheme, using two inverted modulating waves, the load voltage has double the number of pulses per carrier time period, thus doubling the ripple frequency. Now, higher the frequency of unwanted ripple-voltage, easier it is to filter out the ripple current. Also, the load voltage now has three levels ($+0.5E_{dc}$, zero, and $-0.5E_{dc}$). Presence of zero duration reduces the rms magnitude of the overall load voltage (fundamental component along with harmonics), while keeping the magnitude of fundamental component of load voltage same as in the previous case (the rms of the overall load voltage for the two-level waveform equals E_{dc}). Thus the overall distortion of the load voltage waveform is less.

37.4 Generation Of 3-Phase Sine-PWM Waveform

A three-phase inverter, as discussed in Lessons 36, can be used to output a three-phase sine modulated pole-voltage pulses. Switches in each of the three poles of the inverter are individually controlled as per the technique discussed in the previous section. For a balanced three-phase output voltage from the inverter poles, the three sinusoidal modulating signals (one for each pole) must also be balanced three-phase signals. The carrier waveform for all the three poles may remain identical. The fundamental components of individual pole output voltages (for $0< m <1$) will thus be proportional to the corresponding modulating signals. For $m = 1$, the rms magnitude of line-to-line voltage (fundamental component) output by the inverter will be equal to $\frac{\sqrt{3}}{2\sqrt{2}} E_{dc}$ ($= 0.612E_{dc}$). A typical line voltage waveform (difference of two pole voltage waveforms) will appear similar to the line voltage waveform (V_{AB}) shown in Fig.37.3.

37.4 A Typical Circuit For Generation Of PWM Waveforms

As mentioned in the preceding section, a three-phase sine-PWM inverter would require a balanced set of three sinusoidal modulating signals along with a triangular carrier signal of high frequency. For a variable-voltage-variable-frequency (VVVF) type inverter, a typical requirement for adjustable speed drives of ac motors, the magnitude as well as frequency of the fundamental component of inverter's output voltage needs to be controlled. This calls for generation of three-phase balanced modulating signals of variable magnitude and frequency which it may be emphasized, need to have identical magnitudes and phase difference of 120 degrees between them at all operating frequencies.

Generating a balanced three phase SINE waveforms of controllable magnitude and frequency is a pretty difficult task for an analog circuit and hence a mixed analog and digital circuit is often preferred. Fig. 37.4 shows a scheme, in block diagram, where the 3-phase analog SINE waves are generated with the help of EPROMs, D/A converters etc.

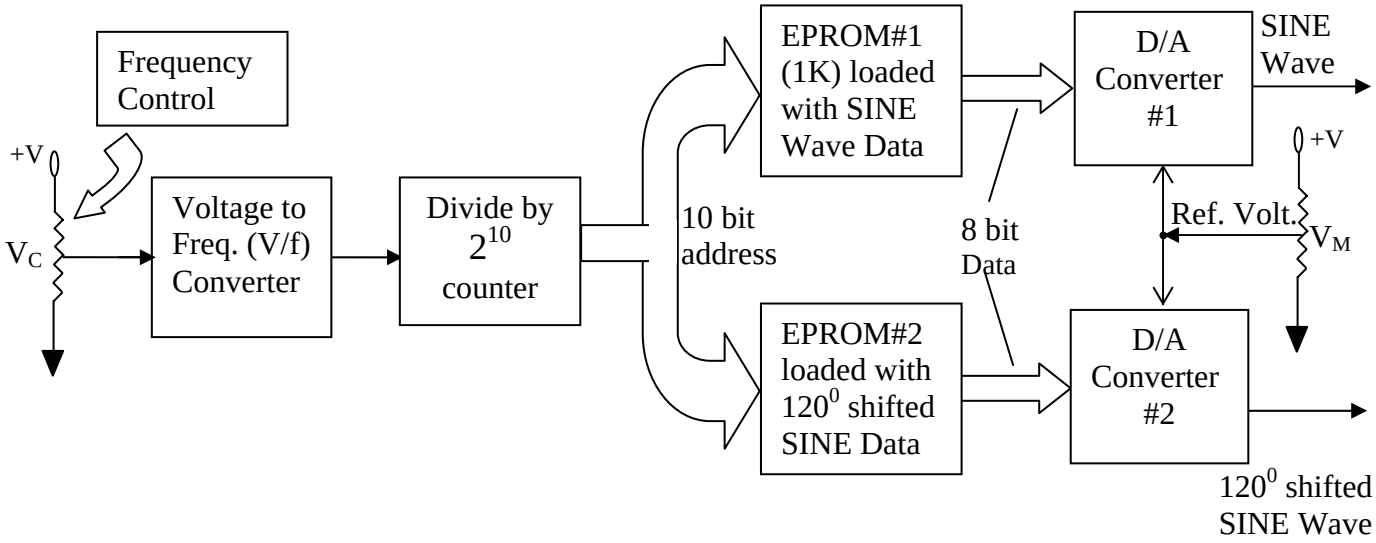

Fig.37.4: Schematic circuit for generation of balanced sinusoidal signals

In the circuit of Fig.37.4, two EPROMs are loaded with discrete values of SINE wave. The first EPROM contains Sin(Φ) values and the second EPROM contains Sin(Φ-120^0) , for $0^0 < \Phi < 360^0$. Let us assume that the EPROMs have 1K (=1024) memory locations. In EPROM#1 Sin(Φ) values are stored serially at discrete but regular intervals of Φ values. Accordingly the first location of EPROM#1 contains Sin(0^0) in digital form, i.e., all the bits are zeroes. The second memory location contains Sin(360^0/1024) in the digital form and so on. Similarly the first memory location of EPROM#2 contains Sin(120^0) and second memory location has Sin(120^0 + 360^0/1024) in digital form. The contents of a particular memory location can be accessed asynchronously by feeding the corresponding address word. A 1K EPROM will have 10 address lines. All address bits, when zero, point to first memory location. As the address word increments the subsequent memory locations are addressed. The EPROMs generally have a 8 – bit word length. Now, Sin(Φ) value, over the full range of Φ, may either be positive or negative. So while digitizing them care must be taken to identify one bit of the word as the sign bit. For example, in the 8 bit (byte length) word the MSB may be used as sign bit with the understanding that if this sign bit is zero the number is positive and if this bit is 1 the number is negative (alternately, one may store '1+ Sin(Φ)' in the memory and the need to store negative numbers will not arise). Leaving one bit (say MSB) as sign bit the 0.0 to 1.0 scale of Sin(Φ) magnitude is divided in 2^7 = 128 equal parts and accordingly the SINE value is digitized. Thus when Sin(Φ) = 1/128 the word to be stored should be 0000 0001. For lesser but positive value of Sin(Φ) the word is 0000 0000. If, for example, Sin(Φ) = -1/64, the word to be stored should be 1000 0010. Here "1" at the MSB location indicates that the number is negative. As seen in the block diagram of Fig.37.4, each EPROM output is fed to a D/A (Digital to Analog) converter to finally come up with analog value of Sin(Φ). Now in the D/A converter, the sign bit is not to be fed. The MSB input of D/A could be grounded. A separate simple logic circuit could take the MSB output of EPROM for sign changing of the D/A output. One such simple arrangement (Fig.37.5) uses an

analog switch, an op-amp and a few resistors to assign correct sign to the analog output of the D/A converter.

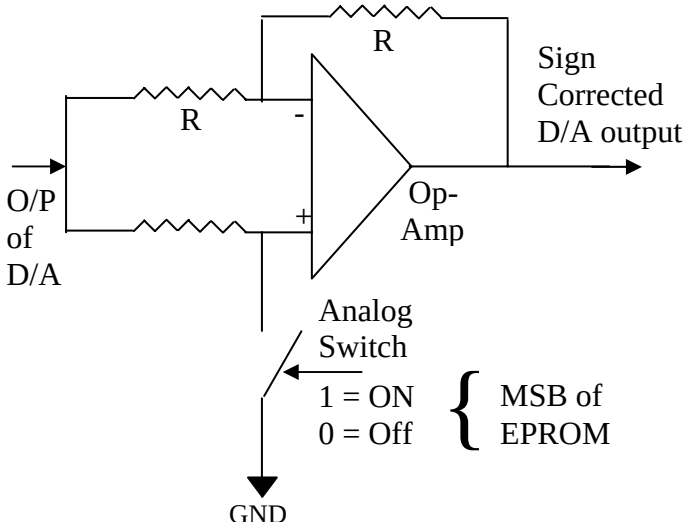

Fig.37.5: A simple sign corrector Circuit

As mentioned earlier, an alternative arrangement for storing data in the EPROM could be to store [1+ Sin(Φ)] value in the memory locations so that negative numbers are not encountered. While decoding the digital value into analog form (using Digital to Analog converter) the analog equivalent of this extra "1" may be subtracted using a simple Op-amp based subtractor circuit.

In the circuit of Fig.37.4, a control voltage V_C is applied to a voltage to frequency (V/f) converter. The V/f converter should preferably have a linear relation between the applied voltage and output frequency. The V/f converter output is fed as clock to a divide by 2^{10} ripple counter circuit. Ten address lines for the 1K EPROM are connected to the ten output lines of the ripple counter. For a 2K EPROM eleven address lines are required and the appropriate counter would then be a divide by 2^{11} counter. The consecutive clock pulses to the ripple counter increment the EPROM's address word sequentially, pointing to the next EPROM memory location after each clock. The EPROM outputs data of the addressed memory location asynchronously. Since the SINE wave data is loaded in the EPROM sequentially, the digital value of SINE wave is output by the EPROM in the correct sequence. The D/A converter then converts the EPROM output into an analog signal. The SINE wave output by D/A converter is however only a stepped approximation of the continuous SINE wave but the number of steps per sine-wave cycle being large (=612), the resolution is sufficient for the present purpose. The Address lines for the two EPROMs are tied together. Thus when, say, first memory location of EPROM#1 is addressed the first location of EPROM#2 is also simultaneously addressed. The SINE waves stored in the two EPROMs are phase shifted by 120^0 and hence the corresponding D/A converters output 120^0 shifted SINE waves. The ten-bit address word generated by ripple counter repeats after 1024 counts and accordingly SINE wave data from the EPROMs are also repeated after 1024 counts (this count represents one output cycle time period of the sinusoidal modulating wave). The rate at which the address bus data changes decides the frequency of the output waveform, which eventually is controlled by the control voltage V_C. D/A converters have reference voltage ($+V_{Ref}$ and $-V_{Ref}$) pins provided for setting the maximum and minimum excursion of the output voltage waveform. In the circuit of Fig.37.4, it is assumed that $-V_{Ref}$ pins are grounded and $+V_{Ref}$ pins are connected to the reference voltage 'V_M'. Thus 'V_M' decides the magnitude of analog

sinusoidal signal output by the D/A converter. The magnitude control signal 'V_M' may be tied to frequency control signal 'V_C' and one may achieve proportional change in inverter's output voltage and frequency. The circuit in Fig.37.4 produces two SINE waveforms having identical magnitude and frequency but phase shifted by 120^0. The third modulating SINE wave could be generated simply by adding these two waveforms followed by a sign inversion. [$\text{Sin}(\Phi) + \text{Sin}(\Phi - 120^0) = - \text{Sin}(\Phi - 240^0)$]. Thus a simple circuit using a couple of op-amps will get the third SINE wave.

High frequency triangular carrier waveform generator and comparator etc. are pretty simple circuits to realize. The comparator output gives the required PWM pattern. The output frequency (as well as magnitude) can be varied in an open-loop or closed-loop by varying the control voltages V_C and V_M.

Quiz Problems

(1) The over-modulation of sine-PWM inverter is generally avoided because it introduces:

(a) lower frequency harmonics in the inverter output waveform
(b) non-linearity between the magnitudes of modulating signal and fundamental voltage output by the inverter
(c) both the above
(d) none of the above

(2) A three-phase sine-PWM inverter operates from a dc link voltage of 600 volts. For modulation index = 1.0 the rms magnitude of line voltage of fundamental frequency will be equal to:

(a) 600 volts
(b) nearly 367 volts
(c) nearly 481 volts
(d) nearly 581 volts

(3) The carrier waveform of a sine-modulated PWM inverter is of 10 kHz frequency. When the fundamental output frequency of the inverter is 50 Hz, the inverter switches need to be turned-on and turned-off at a rate of

(a) 1000 times per second
(b) 10,000 times per second
(c) 50,000 times per second
(d) 50 times per second

(4) A three-phase sine-modulated PWM inverter is used to get a balanced 3-phase fundamental output voltage. The modulating waveforms must have

(a) Three DC signals of identical magnitude
(b) Three balanced ac signals of fundamental frequency
(c) Three identical and in-phase ac signals of fundamental frequency
(d) Three balanced ac signals of carrier frequency

Answers to Question Problwm: 1-c, 2-b, 3-b, 4-b.