Pulse Skipping Modulated DC to DC Step Down Converter Under Discontinuous Conduction Mode

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Abstract—Reduced switching loss favours Pulse Skipping Modulation mode of switching dc-to-dc converters at light loads. Under certain conditions the converter operates in discontinuous conduction mode (DCM). Inductor current starts from zero in each switching cycle as the switching frequency is constant and not adequately high. A DC-to-DC buck converter is modelled and simulated in this paper under DCM. Effect of ESR of the filter capacitor in input current frequency components is studied. The converter is studied for its operation under input voltage and load variation. The operating frequency is selected to be close to and above audio range.

Keywords—Buck converter, Discontinuous conduction mode, Electromagnetic Interference, Pulse Skipping Modulation.

I. INTRODUCTION

SWITCHING DC-to-DC buck converters find application where a source voltage is higher than that required by the load. A buck regulator operates with higher efficiency and maintains the output voltage at desired level and used when there are possibilities of variations in input voltage or load. In a voltage mode PWM controller, the duty cycle is altered, based on error between set voltage and measured output voltage so that the output voltage of the converter is very nearly equal to the desired value [1]. The resulting PWM voltage wave is filtered with LC network to derive the required DC voltage.[2]. Apart from maintaining the line and load regulations low, it is also desirable to retain the losses low especially in portable applications with energy-limited sources. It is desirable that the efficiency is kept high throughout the operating range. Efficiency of PWM switching regulators is in general high compared to linear regulators but not constant over the entire load range [3]. Efficiency of a PWM regulator at light load is considerably less in comparison with that at near full load conditions. The problem is pronounced at low voltage portable applications. Various topologies and methods of control were suggested and synchronous buck topology with ZVS technique is suggested for minimizing switching losses [4] - [6]. The Efficiency of synchronous converter can be further improved with low side MOSFET device that includes Schottky diode integrated [7].

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To improve the efficiency at light loads during stand by mode, several techniques including improved controllers with digital PWM, PFM with reduced switching and conduction losses were proposed [8] - [10]. Pulse Skipping Modulated Converters operate with higher efficiency at light loads with reduced switching loss due to pulse skipping [11]. A pulse skipping modulated dc-dc converter under certain conditions operate in discontinuous conduction mode where the inductor current starts from zero every switching cycle. A PSM converter under discontinuous conduction mode is modeled and simulation results are given.

II. PULSE SKIPPING MODULATED BUCK CONVERTER

A pulse skipping modulated buck converter shown in Fig.1, essentially consists of a MOSFET switch, a diode, an inductor L, and a capacitor C. L and C filter out the ripple and designed suitably so that the LC filter cut off frequency is well below the switching frequency. The feedback circuit consists of a PSM control logic, which allows the pulse generated by the clock if actual voltage is below a lower threshold value and skips pulses if the actual voltage goes above the upper threshold value.
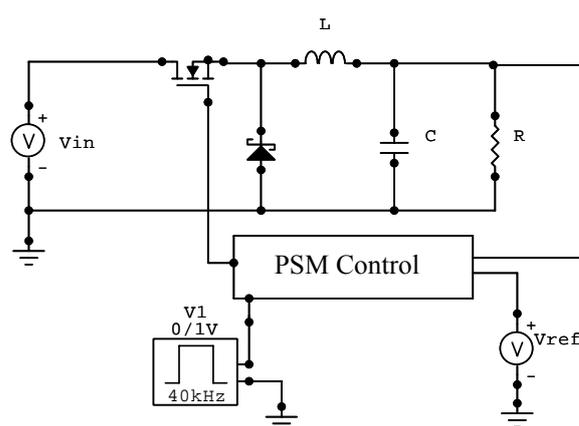

Fig. 1 Pulse Skipping Modulated Buck Converter

The clock pulse generated is a constant frequency constant width (CFCW) pulse. MOSFET switch is ON when the clock pulse is applied over a fixed duration of time depending on duty cycle of the clock and the inductor current rises linearly.

The switch is OFF for the remaining period of the cycle and the current drops to a lower value. In the case of discontinuous conduction the current drops to zero and remains zero till the next cycle. In the case of continuous conduction mode it drops to a lower value, which is higher than the initial value of the cycle. Alternately permitting p pulses and skipping q pulses maintain the output voltage at a value between upper and lower reference values. The waveforms are shown in Fig.2 for discontinuous conduction.
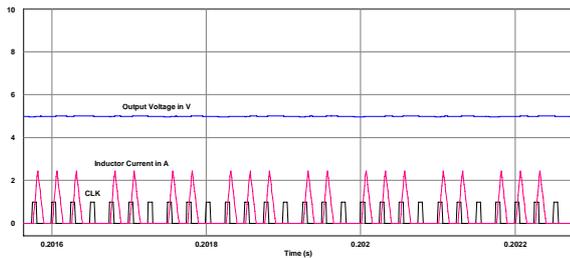

Fig. 2 Waveforms of Inductor current, output voltage, and gate pulses for a PSM converter.
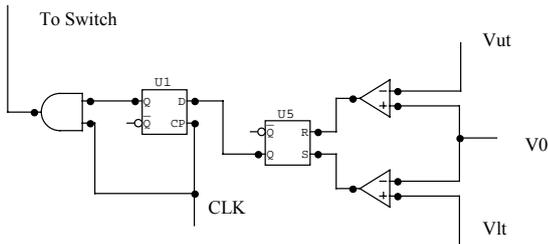
III. PSM CONTROL LOGIC

Fig 3 Control Logic

As shown in Fig 3 the output voltage v0 is compared with lower and upper threshold values. When v0 drops lower than Vlt lower comparator output sets the flip-flop making Q HIGH. This in turn makes Q output of the D flip-flop HIGH by the next clock cycle and the clock pulses are applied to the switch through the AND GATE from then on. When v0 rises and goes higher than Vut, upper comparator output resets the flip-flop making Q LOW that in turn makes D input LOW. This makes D flip flop output LOW from next clock cycle and the clock pulses do not pass through AND GATE and hence the pulses are not applied to the switch and are skipped till v0 again becomes less than Vlt. This way the output voltage is maintained at a value close to the reference value.

IV. MODELING OF PSM CONVERTER UNDER DCM

The converter is assumed to work in discontinuous Conduction Mode (DCM). The converter can be modeled using State Space Averaging technique [12], [13]. Let for p cycles the clock pulses are applied and for q cycles the pulses are skipped for a particular load resistance R and input voltage Vin. The duration pT is known as charging period and the duration qT is known as skipping period. During the charging period, in each cycle the switch is ON for duration equal to D1T and OFF for duration equal to (1 − D1) T. During this period inductor current drops to zero in D2T and hence the current is zero during the remaining (1 − (D1 + D2)) T. During the skipping period the switch is OFF throughout as the pulses are not applied and skipped.

The state space equations, assuming discontinuous conduction mode with rC<<R are obtained as:

During charging period,

$$\dot{x} = A_1 x + B_1 u \qquad 0 \le t \le D_1 T$$
$$y = C_1 x \tag{1}$$

$$\dot{x} = A_2 x + B_2 u \qquad D_1 T \le t \le (D_1 + D_2)T$$
$$y = C_2 x \tag{2}$$

$$\dot{x} = A_3 x + B_3 u \qquad (D_1 + D_2)T \le t \le T$$
$$y = C_3 x \tag{3}$$

During skipping period,

$$\dot{x} = A_3 x + B_3 u \qquad 0 \le t \le T$$
$$y = C_3 x \tag{4}$$

Where,

$$A_1 = A_2 = A = \begin{bmatrix} -\dfrac{r_C}{L} & \dfrac{-1}{L} \\ \dfrac{1}{C} & 0 \end{bmatrix} \tag{5}$$

$$A_3 = 0 \tag{6}$$

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{7}$$

$$u = \begin{bmatrix} v_{in} \\ i_0 \end{bmatrix} \tag{8}$$

$$y = \begin{bmatrix} v_0 \\ i_{in} \end{bmatrix} \tag{9}$$

$$B_1 = \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_C}{L} \\ 0 & -\dfrac{1}{C} \end{bmatrix} \tag{10}$$

$$B_2 = \begin{bmatrix} 0 & \dfrac{r_C}{L} \\ 0 & -\dfrac{1}{C} \end{bmatrix} \tag{11}$$

$$B_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{C} \end{bmatrix} \quad (12)$$

$$C_1 = \begin{bmatrix} r_C & 1 \\ 1 & 0 \end{bmatrix} \quad (13)$$

$$C_2 = \begin{bmatrix} r_C & 1 \\ 0 & 0 \end{bmatrix} \quad (14)$$

$$C_3 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \quad (15)$$

Defining Modulation Factor M,

$$M = 1 - \frac{f_a}{f} \quad (16)$$

$$\frac{f_a}{f} = \frac{p}{p+q} \quad (17)$$

Where,

f_a – Actual frequency of switch

f – Clock frequency

After State Space Averaging,

$$\dot{x} = \left[(1-M)\left\{ A(D_1 + D_2) \right\} \right] x + \left[(1-M)\left\{ (B_1 - B_3)D_1 + (B_2 - B_3)D_2 \right\} + B_3 \right] u \quad (18)$$

$$y = \begin{bmatrix} r_C(D_1 + D_2) & 1 \\ D_1 & 0 \end{bmatrix} x \quad (19)$$

V. SIMULATION

Simulation of the PSM DC-DC buck converter was carried out with the following parameters. Vin = 12V to 20V, V0 =5V, L = 16µ H, C=470µ F, ESR = 5mΩ, f=40KHz.

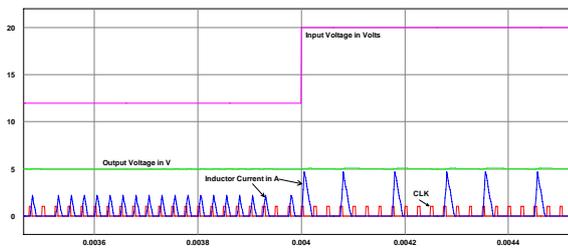Pulse skipping increased to regulate the output voltage with increase in input voltage as shown in Fig 4.

Fig. 4 Output voltage for step increase in input voltage

Input voltage was stepped up from 12V to 20V and the output voltage was plotted. Output voltage waveform for a constant load with a step increase in input voltage is shown along with applied pulses and inductor current indicating discontinuous conduction.

Response showed that PSM converter can accept wide variations in input voltage and its response speed was good as seen from step response and the output voltage was regulated over the entire range. Modulation Factor increased with Increase in voltage increasing the pulses skipped.
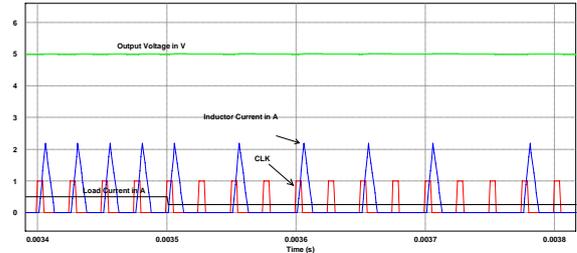

Fig. 5 Output voltage for step decrease in load current

Load was decreased by a step from 0.5A to 0.25A and the output voltage is shown in Fig.5 Pulses skipped increased, as load was decreased to regulate the voltage. The ripple of the output voltage was higher as input voltage was increased. A similar response was observed when the load was decreased.

Input current harmonic spectrum of the PWM converter is shown in Fig 6 and that of PSM converter is shown in Fig 7 for comparison purpose for the same input voltage and load.
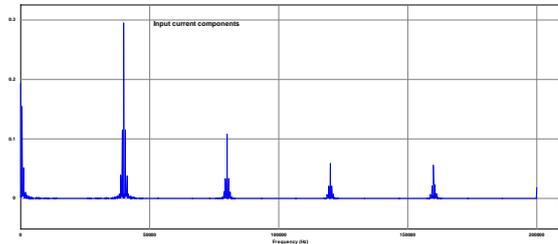

Fig. 6. Input Current Harmonic Spectrum - PWM Converter

PSM converter exhibits better EMI performance [14] with individual frequency components smaller than those of PWM converter. In the case of PSM converter harmonic components are spread over a wide band of frequencies lowering the average value of the peaks of currents. Due to reduction in average frequency with pulse skipping at light loads there are components entering into audio frequency range as shown in Fig 7 which may result in audible noise interference, which can be avoided through filtering along with proper selection of switching frequency.
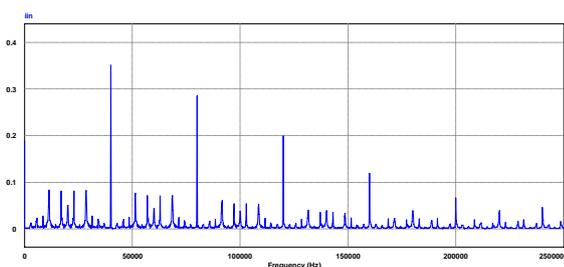
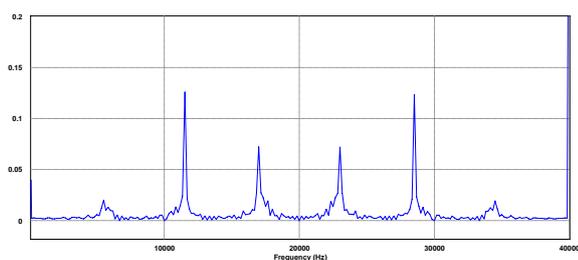Fig. 7. Input Current Harmonic Spectrum - PSM Converter

Fig. 8. Input Current Harmonic Spectrum - Audio Frequency Range – PSM Converter

Fig 8 shows the frequency components of input current over 0 to 40 kHz for filter capacitor ESR of 5 mΩ. Increase in ESR decreases the number of components in audio range but switching frequency harmonic components were found to be higher in magnitude.

VI. CONCLUSION

Pulse Skipping Modulated Buck converter was modeled and simulated under discontinuous conduction mode. Response of the converter for input voltage and load step variation was studied. The converter response to changes was quick and the PSM controlled converter regulated the output voltage over the entire range of input voltage intended for operation. Increase in input voltage was followed by increase in Inductor current peak value and was considerably high. With ESR not neglected the output voltage ripple increases Input current harmonic spectrum was studied and compared with that of PWM controlled Converter. PSM converter has a well spread out spectrum, with individual component peak values less in amplitude, making its EMI performance better than that of PWM controlled converter. But there are frequency components entering into audio frequency range due to the average frequency of switching being lower with pulse skipping, if the switching frequency is selected to be just above the audio range. ESR of the capacitor affects the spread of frequency components and their magnitude. Number of components decrease with increase in their magnitude.

REFERENCES

[1] Erickson, R. W., Maksimovic, D., Fundamentals of Power Electronics, Kluwer Academic Publishers, 2nd Edition, ISBN 0-7923-7270-0.

[2] A. J. Stratakos, S. R. Sanders, and R. W. Broderson, "A low-voltage CMOS dc–dc converter for a portable battery-operated system," in Proc. Power Electronics Specialists Conf., vol. 1, June 1994, pp. 619–626.

[3] Angkititrakul, S.; Hu, H.; "Design and analysis of buck converter with pulse-skipping modulation," Power Electronics Specialists Conference, 2008. PESC 2008. IEEE , vol., no., pp.1151-1156, 15-19 June 2008. doi: 10.1109/PESC.2008.4592085

[4] Angel V.Peterchev, Seth R.Sanders, "Digital Loss –Minimizing Multi-Mode Synchronous Buck Converter Control"35th Annual IEEE Power Electronics Specialists Conference, pp.3694-3699

[5] S. Pattnaik, A. K. Panda, Aroul K., K. K. Mahapatra, "A Novel Zero Voltage Transition Synchronous Buck Converter for Portable Application," International Journal of Electrical, Computer, and Systems Engineering, Volume 2 Number 2 pp. 115–120 Spring 2008.

[6] A. Consoli, F. Gennaro, C. Cavallaro, and A. Testa, "A comparative study of different buck topologies for high-efficiency low-voltage applications," in Proc. Power Elect. Spec. Conf., 1999, pp. 60-65.

[7] Calafut, D., "Trench power MOSFET lowside switch with optimized integrated Schottky diode," Proceedings of The 16th International Symposium on Power Semiconductor Devices and ICs, 2004. ISPSD '04., vol., no., pp. 397-400, 24-27 May 2004.

[8] K.M.Smith and K.M.Smedly, "A comparison of voltage-mode soft switching methods for PWM converters," IEEE Trans. Power Electron., vol.12, no.2, pp.376-386, Mar.1997.

[9] Xunwei Zhou, Mauro Donati, Luca Amoroso, and Fred C. Lee," Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," IEEE Transactions On Power Electronics, Vol. 15, No. 5, pp.826-834, September 2000

[10] Chi-Lin Chen Wei-Lun Hsieh Wei-Jen Lai Ke-Horng Chen and Ching-Sung Wang," A new PWM/PFM control technique for improving efficiency over wide load range, " 15th IEEE International Conference on Electronics, Circuits and Systems, 2008 pp 962-965.

[11] Luo P,Luo L Y, Li Z J et al,"Skip Cycle Modulation in Switching DC-DC Converter", ICCCAS, Chengdu, China,June, 2002, 1716-1719.

[12] Luo Ping, Zhang Bo,Wang Shun-Ping, Feng Yong,"Modeling and Analysis of Pulse Skip Modulation" Journal of Electronic Science and Technology of China, March 2006, Vol 4(01).

[13] Middlebrook, R.D., Ćuk, S. A general unified approach to modeling switching-converter power stages. Int. Journal of Electronics, Vol 42, No. 6, 1977, pp. 512-550.

[14] A. Farhadi, A.Jalilian,"Modeling, Simulation and Reduction Techniques of Electromagnetic Conducted Emission Due to Operation of Power Electronic Converters", International Conference on Renewable Energy and Power Quality (ICREPQ'07), Sevilla, Spain, March 2007.W.-K. Chen, Linear Networks and Systems (Book style). Belmont, CA: Wadsworth, 1993, pp. 123–135.