**Printed circuit boards-Track resistance**

The resistance of PCB tracks varies in proportion to their length and inversely to their cross-sectional area. The track resistance R is given by the formula:

$$R = \frac{\rho \cdot L}{A}$$

where

ρ = the volume resistivity of the conductor (approximately 1.72 × 10−6 Ω·cm)

L = the length of the conductor

A = the cross-sectional area of the conductor

This formula gives a reasonable estimate for the resistance of a wide track, but few narrow tracks have vertical sides. A better estimate of the shape is given by Figure 1, which shows a trapezoidal cross-section, where the undercut on each side is approximately half the thickness of the track.

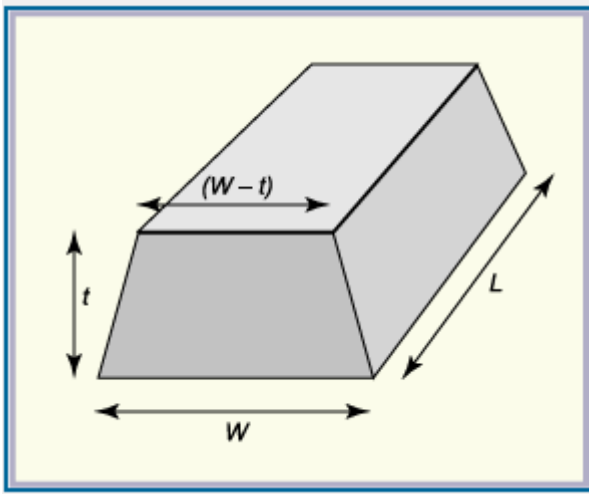


Figure 1: Trapezoidal cross-section of a track on a PCB

Using this approximation, the area of the cross-section of the track can be estimated using the formula:

$$A = \left[(w - t) \times t\right] + t^2/2$$

The thickness of the copper of course is the actual thickness of foil, together with any plating, allowing for the thickness tolerance on both plating and initial foil.

Copper also has a substantial positive temperature co-efficient of resistance which may need to be taken into consideration if there is substantial track heating. For more information on calculating DC line resistance, see http://www.merix.com/resourcecntr/tech/dc_line.doc

Whilst for digital signals even the thinnest tracks that can be manufactured consistently and economically are more than adequate to carry the signal current, current-carrying capacity has to be considered on high dissipation boards. This is especially important with multilayer boards, which have higher track concentrations, and where tracks on inner layers cannot radiate heat direct to the air.

The current-carrying capacity of a track depends on its width and the thickness of the copper foil from which it was etched, and on the permissible heat rise, which is a complex function of materials, construction, operating temperature range and intended use. Figure 2 is a typical set of curves that shows how the steady state temperature rise in a 70 µm thick copper foil is related to current and track width.

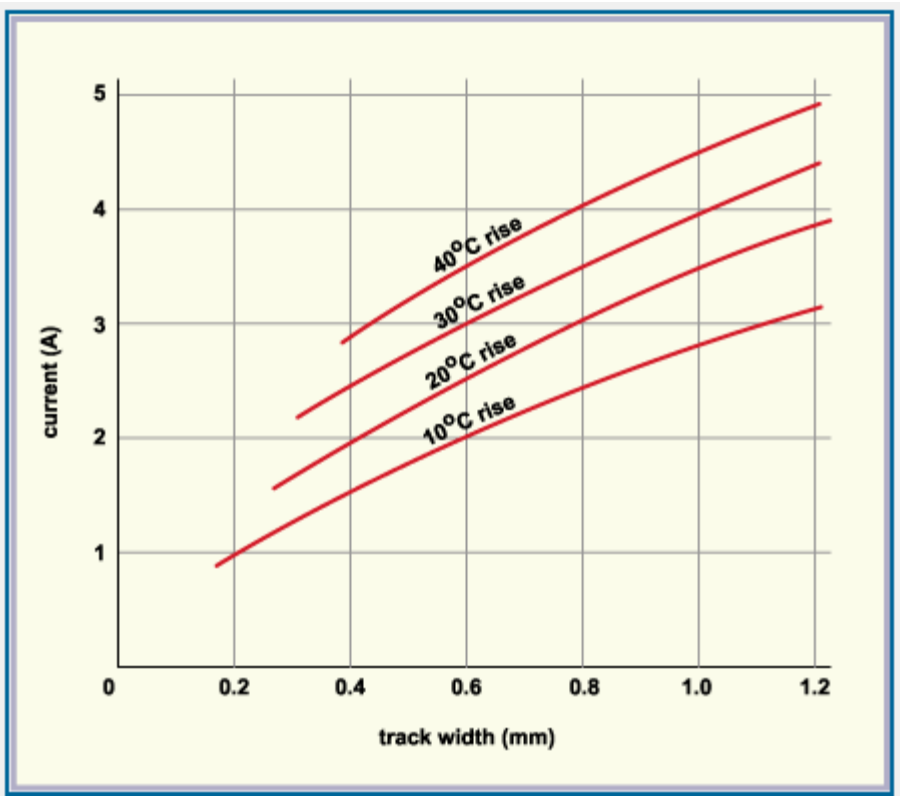


Figure 2: Heat rise in a 70 µm copper foil as a function of current and track width

IPC-2221 contains a fuller set of such curves, which may be used to calculate the recommended track width for any current. Obviously, in assessing what track temperature rise is allowable, the designer has to take into account the maximum operating temperature of the laminate and the worst case internal temperature of the equipment. The ways in which the full chart can be used, and a copy of the charts themselves is available at the UltraCAD website at http://www.ultracad.com/using_ipc_temp_charts.pdf

The charts rely on graphical interpolation, which is not terribly convenient, so you may like to try one or more of the calculators that are aimed to help the designer relate current, conductor width, and conductor thickness. They vary considerably in ease of use and sophistication:

Doug Brooks: http://www.ultracad.com/calc.htm

Parlin: http://www.parlin.com/tools.htm

Minnitron: http://www.minnitron.co.uk/calc.htm

Brad Suppanz:
http://www.geocities.com/CapeCanaveral/Lab/9643/TraceWidth.htm

The first two of these are downloads; the others are Javascript calculators that can be run from your browser; all are based on IPC-2221.

Whilst the graphs seem fairly clear in their recommendations, practical experience has indicated that the results they yield are far from accurate. Fortunately conservative, they prove to be based on very old experiments indeed, even before the days of multilayer, so that their extension for use with internal layers was based on pure hypothesis! Nevertheless, they are still the official IPC position. Until, that is, when the new standards, more closely aligned to experiment results, are released. Work on this is reported by IPC under IPC-2152, a standards development committee chaired by Mike Jouppi. Information on this, based on Mike's work, has been made available by Coretec, and may be accessed at this link (PDF file, 358KB).

But what do you do in a high-power application, when the calculator suggests that, to avoid over-heating and possible damage, a wider track should be used than can be fitted into the space available? The main alternatives are either to select a laminate with a thick copper foil or to increase the track thickness locally by selective plating. In some high-current cases, it may be advantageous to fit bus-

bars as components: bear in mind that resistive heating is associated with voltage drop, and this may also impact on circuit performance.

Ground and power connections are usually planes, complete layers of copper connected either to ground or supply voltage. This minimises both the resistance and the inductance of the connection, although the plane is less than perfect because it is pierced with multiple holes. One problem area is getting high currents into a plane: designers must have a sufficient total cross-sectional area of copper in contact with the connector pin(s), and this depends on their number and diameter, as well as the foil parameters.

Contact resistance points on the board, such as an edge connector, may be coated with thicker gold to provide a low resistance connection which can be made and broken during life. This coating is totally different from the electroless nickel with gold flash used for soldering, that we will discuss in later parts of this unit. It typically consists of electrolytically-deposited hard nickel covered with 1-3 μm of hard gold, so that the design has to allow for electrical connection to be made to these areas during the plating operation. The practicalities of this are beyond the scope of this module, and you should consult your board fabricator.

Author: Martin Tarr

**Source: http://www.ami.ac.uk/courses/topics/0185_tr/index.html**