Optimizing the Number of Bits/Stage in 10-Bit, 50Ms/Sec Pipelined A/D Converter Considering Area, Speed, Power and Linearity

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***Abstract*—**Pipeline ADCs are becoming popular at high speeds and with high resolution. This paper discusses the options of number of bits/stage conversion techniques in pipelined ADCs and their effect on Area, Speed, Power Dissipation and Linearity. The basic building blocks like op-amp, Sample and Hold Circuit, sub converter, DAC, Residue Amplifier used in every stage is assumed to be identical. The sub converters use flash architectures. The design is implemented using 0.18μm CMOS technology and uses 3.3V power supply. The paper implements a 10 bit 50MSPS pipelined ADC using 1, 1.5, 2, 3, 4 and 5 bits/stage conversion and compares them with respect to Area, Speed. Power and Linearity. The paper concludes by stating that 2bits/stage is optimum for a pipelined ADC and to reduce design complexity we can go up to 3 bits/stage.

***Keywords*—**1.5 bits/stage, Conversion Frequency, Redundancy Switched Capacitor Sample and Hold Circuit.

I. Introduction

THE rapidly growing electronics has resulted in digital revolution with telephony switching systems in 1970's and continued with digital audio in 1980's and digital video in 1990's. This is expected to prevail in the present multimedia era and even can influence in future systems. Since all electrical signals in nature are analog and since most signal processing is done in the digital domain therefore, A/D and D/A converters have become a necessity. Successive approximation ADC makes single bit decision at a time while flash ADC makes all bit decisions in a single go. Successive approximation ADC is slow and occupies less area while flash ADCs are faster but area increases exponentially with bit length.

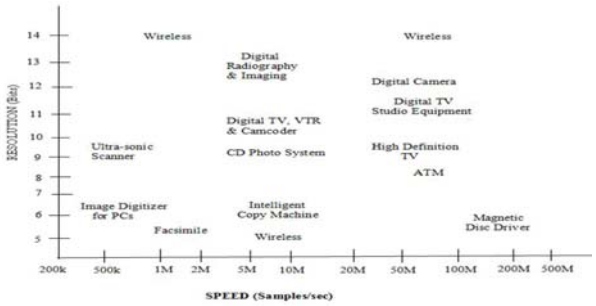

Fig. 1 Speed versus Resolution

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Between these two extremes many other architectures exist deciding a fixed number of bits at a time such as pipeline and multistep ADCs. They balance speed and circuit complexity. Fig. 1 shows recently published high speed ADC resolution versus speed. For example, over sampling converter is used exclusively to achieve high resolution (greater than 12 bits at low frequencies). For medium speed with high resolution multi step and pipeline ADCs are promising. At extremely high frequencies, only flash ADCs survive but with a low resolution.

Fig. 2 shows resolution versus speed showing this trend. Most architectures known to date are not likely to achieve a resolution of 12 bit at over 100 MHz using even 180 nm to 90 nm technologies. However, two high speed architectures, namely multi step, pipelined and folding are potential architectures to challenge in times to come.

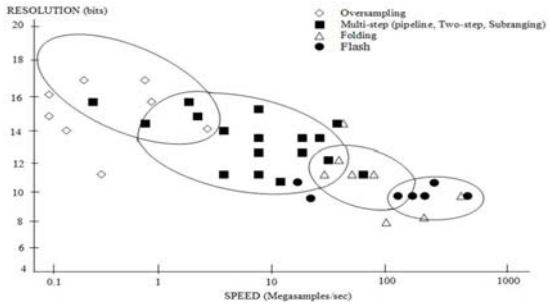

Fig. 2 Performance of recently published ADCs

A. Flash ADC

Comparing the input with all divided levels of the reference voltage is the straightforward approach and this is used in flash ADC. The conversion completes in a single step. Therefore, flash ADC is the fastest of all ADCs. Fig. 3 shows flash ADC technique.

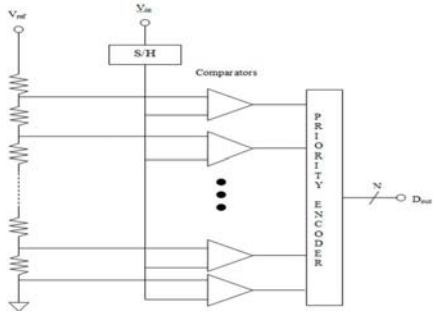

Fig. 3 Flash ADC Architecture

The priority encoder is required as the output of comparator set is thermometer coded. The performance is decided by the accuracy of voltage divisions and the comparator resolution. Practically, the exponential growth of the number of comparators and resistors with increased bit size limits the usage of flash ADCs. An N bit flash ADC requires 2^{N-1} comparators and 2^N resistors. Also with increased bit length, the comparators present significant capacitive loading on the Sample and Hold circuit thus reducing the speed of conversion. The power consumption also becomes high as capacitive loading and comparators number increases. Therefore, flash converters are preferred where the bit length is less than 8, flash ADCs are preferred as coarse and fine quantizers in multi step and pipeline ADCs.

B. Multi Step ADC

Instead of making single bit decision at a time as in successive approximation ADC or making all bit decisions at a time as in flash ADC, we can resolve a few bits at a time as it makes the system simpler and easily manageable. It also allows us to use digital error correction mechanism. This is adopted by the multi step ADC architecture. Here only a single Sample and Hold circuit is used and every stage requires a coarse ADC, DAC and a residue amplifier as shown in Fig. 4. To complete conversion in one clock cycle, we need to use multi phase clocking scheme. The difficulty in clocking makes the multi step architecture to limit the number of steps to two. Also it doesn't reduce speed much and can use standard two phase clocking.

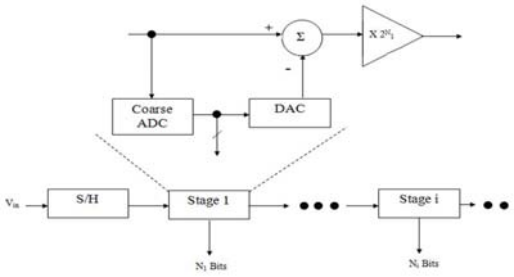

Fig. 4 Multi step ADC Architecture

C. Pipeline ADC

Although simpler and manageable, the complexity of two step ADC still grows exponentially as the number of bits/stage increase. For resolution of 10 bits and above, the complexity reaches a maximum and hence the need for pipelining the sub ranging blocks arises. Fig. 5 shows the pipeline ADC architecture. It looks similar to multi step ADC architecture except that every stage uses a separate sample and hold circuit. Since Sample and Hold circuits are clocked by alternating clock phases, in every clock phase, a stage must perform the bit decision and amplify the difference signal to generate the residue for the next stage. Pipelining the residue greatly simplifies the ADC architecture. The complexity now grows linearly with the number of bits to resolve and hence is becoming popular. Here the accuracy of the residue amplifier limits the overall performance. The potential error sources are ADC/DAC resolution, gain error of residue amplifier and the settling behavior of the amplifier.

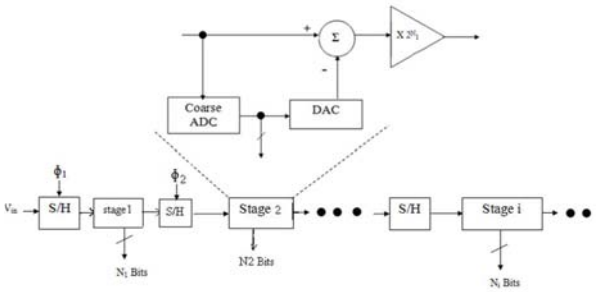

Fig. 5 Pipeline ADC Architecture

II. Pipeline ADC Types

This paper discusses the options of number of bits/stage conversion techniques in pipelined ADCs and their effect on area, speed, power dissipation and linearity. The paper examines 1, 1.5, 2, 3, 4 and 5 bits/stage conversion to implement a 10 bit pipelined ADC. In the analysis, all the basic blocks are assumed to be identical.

A. One Bit Per Stage Pipeline ADC

The degenerate case of pipeline ADC is when only a single bit is resolved per stage as shown in Fig. 6. Each stage here performs the following operation.The sampled signal is compared with Vref/2 and the output of each comparator becomes the converted bit for that stage.

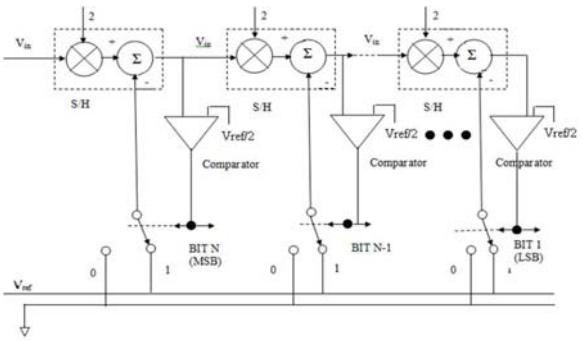

Fig. 6 One bit/stage Pipeline ADC Architecture

If Vin > Vref/2, the output of comparator = '1', then Vref/2 is subtracted from the held input signal and the difference is passed to the amplifier. The residue from the subtractor is multiplied by 2 and the result is passed as input to Sample and Hold circuit of the next stage.

In pipeline ADC architecture, the MSB stage must be carefully designed. A slight error in first stage propagates through the converter and hence can result in a much bigger error at the end of conversion. The succeeding stages can be less accurate. The comparator and summer offsets together must be less than ½ LSB to keep the ADC accurate.

B. 1.5 Bits/Stage Pipeline ADC

Pipelined ADCs get their final resolution using cascaded lower resolution stages [3] [8] [9]. For example, a 12 bit ADC

can use a cascade of four 3-bit stages. Many designers are comfortable with 3-bit flash ADCs. However, 1.5 bits / stage is also becoming increasingly popular. For high speed converters there is an advantage of going for minimum stage resolution. It minimises the inter stage gain required, which in turn maximises the bandwidth, since gain bandwidth product is a constant for a given technology.

A 1.5 bits/stage is a 1bit/stage into which some redundancy is added to compensate for device tolerances and imperfections [11]. A digital error correction mechanism later eliminates this redundancy. The 1.5bits/stage uses two analog comparison levels Vu & VL instead of a single level as in 1 bit/stage. Because of the use of gain of two, they must lie between –Vref/2 and +Vref/2. A common choice is Vu = +Vref/4 and VL = – Vref/4. The MDAC architecture and its voltage transfer characteristics are shown in Fig. 7 which is highly nonlinear. The input voltage range is divided into three sections. The low range (L) below V_L, mid range (M) between Vu and V_L and the upper range (U) above Vu, and as shown in the Table I. The implementation details of 1.5bits/stage is shown in Fig. 7 (a). A resistor string provides voltage division to create reference voltages Vu and V_L.

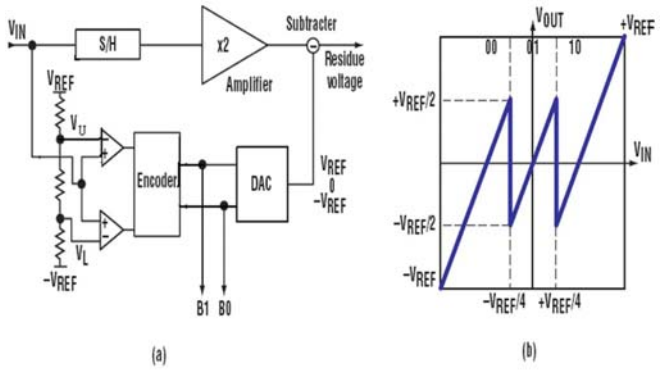

Fig.7 a) MDAC for 1.5 bit conversion b) transfer characteristic

All other high accuracy operations such as multiply-by-two are achieved by capacitor ratios. The multiply-by-two amplifier and sample and hold circuit can be combined to form a multiplying DAC (MDAC). The cascaded MDAC outputs are passed through latches before feeding the redundancy bit removal circuit as shown in Fig.9.

1. Redundancy Bit Removal Algorithm

The probable error sources in data converters include gain error in amplifier and offset voltages in comparators and op-amps, nonlinearity in converter and others. Many of these errors are compensated by the redundancy bit removal algorithm [8] [9].

TABLE I
BIT GENERATION DETAILS OF MDAC

Vin	Range	B_1	B_0	DAC output	Analog residue output
Vin>Vu	U	1	0	+ Vref	2Vin–Vref
V_L<Vin< Vu	M	0	1	0	2Vin
Vin< V_L	L	0	0	- Vref	2Vin+Vref

Each 1.5bit pipelined stage produces a 2 bit output code B_1B_0. Using redundancy bit removal algorithm, this is reduced to final 1 bit per stage code. For a resolution of 3 bits, the input voltage range of ±2V is divided into 8 equal slots and Table II shows input voltage, the code generation of each stage and corresponding stage residue voltages. To generate the final code, the two bit codes generated by each stage are added in a predetermined way. For example, as highlighted in Table II, for Vin = 1.23V, the codes generated by successive stages are 10, 01 and 10. These bits must be added as follows to generate the final 3 bit code.

```
  1  0
+ 0  1
+    1  0
  ---------
  1  1  0  0
  ---------
```

Discard LSB and the final digital code is 110 for the case Vin = 1.23V.

TABLE II
DEVELOPMENT OF ERROR CORRECTED OUTPUT CODE

VIN (V)	RANGE (1)	CODE (1)	RES (1)	RANGE (2)	CODE (2)	RES (2)	RANGE (3)	CODE (3)	OUTPUT CODE
1.80	U	10	1.60	U	10	1.20	U	10	111
1.23	U	10	0.46	M	01	0.92	U	10	110
0.80	U	10	-0.40	M	01	-0.80	L	00	101
0.30	M	01	0.60	U	10	-0.80	L	00	100
-0.26	M	01	-0.52	L	00	0.96	U	10	011
-0.70	L	00	0.60	U	10	-0.80	L	00	010
-1.30	L	00	-0.60	L	00	0.80	U	10	001
-1.60	L	00	-1.20	L	00	-0.40	L	00	000

The circuit implementation is shown in Fig. 8.

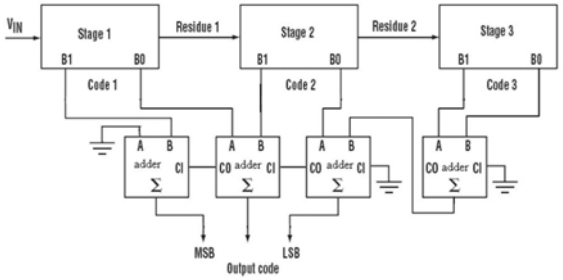

Fig. 8 Implementation of redundancy bit removal algorithm

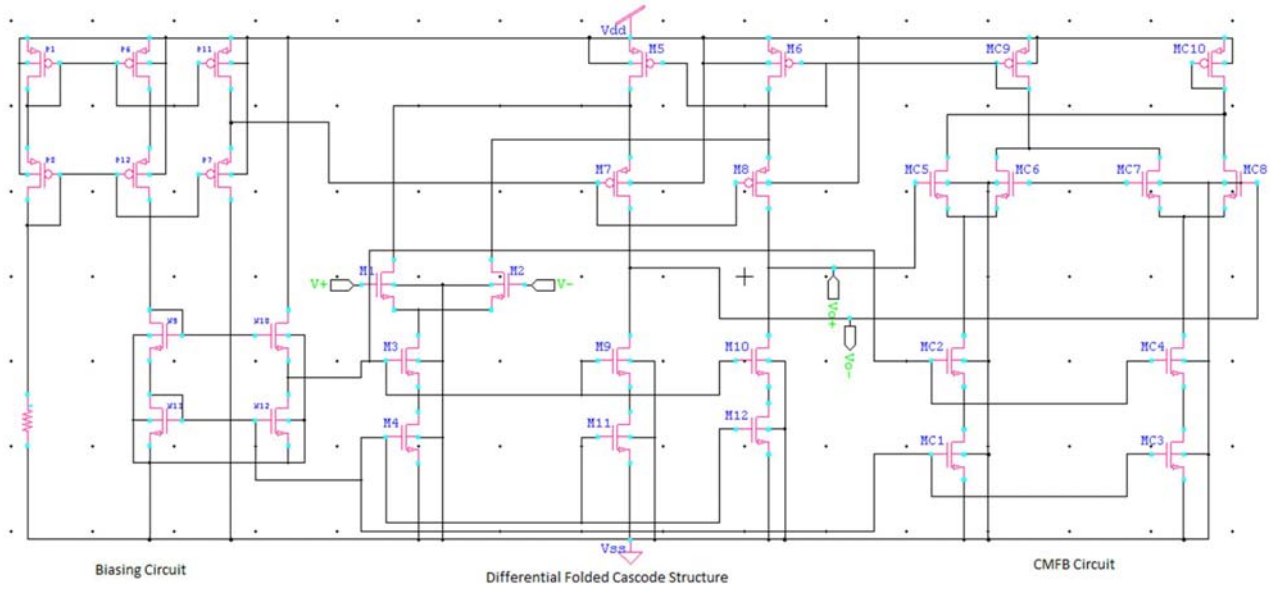

Fig. 9 Folded cascode Operational Amplifier

C. 2 Bits /Stage And Above

With 2 bits/stage, the 10 bit pipelined ADC is implemented using 5 stages and with 3 bits/stage, it uses 4 stages converting, 3, 3, 3 and 1 bit respectively in consecutive stages [12]. Using 4 bits/stage conversion the ADC is implemented in 3 stages converting 4, 4, 2 bits in successive stages and so on. All the sub converters are implemented using flash architectures already discussed.

III. Implementing The Pipelined ADCs

The various building blocks used are discussed here. The same blocks are used in different bits/stage conversions and the analysis is done with respect to area, speed of conversion, power dissipation and linearity.

A. Folded Cascode Op-Amp

Driving capacitive loads is the trend in Modern integrated CMOS op-amps. With capacitive load, it is not necessary to use a buffer at the output (for providing a low impedance node). Therefore, it is possible to design op-amps at larger voltage swings and higher speeds than those which drive pure resistive loads [4] [5] [6]. These improvements are achieved with a single high impedance node at the output that drives only capacitive loads. For folded cascode op-amps the compensation is achieved by load capacitance CL itself and it provides dominant pole compensation. As CL increases, the op-amp stability improves but gets slowed down. The schematic of folded cascode op-amp is shown in Fig. 9. The basic idea of folded cascode op-amp is to apply the opposite type PMOS cascode transistors to the input differential pair of NMOS type.As supply voltages and transistor channel lengths are scaled down, the design of op-amp is becoming increasingly difficult. There are several op-amp topologies possible viz.

Two stage CMOS op-amp, Regulated cascode op-amp, folded cascode op-amp and Telescopic cascode op-amp etc. A two stage CMOS op-amp is preferred where high gain and large output swing are required. However, the addition of second stage reduces unity gain frequency and hence speed of operation. A telescopic cascode op-amp offers better power and BW criterion but has severe drawback of reduced output swing and hence not preferred for low voltage applications. Folded cascode op-amp provides higher output swing compared to telescopic cascode op-amp and better PSRR and speed over two stage op-amp. Hence folded cascode op-amp is used here.

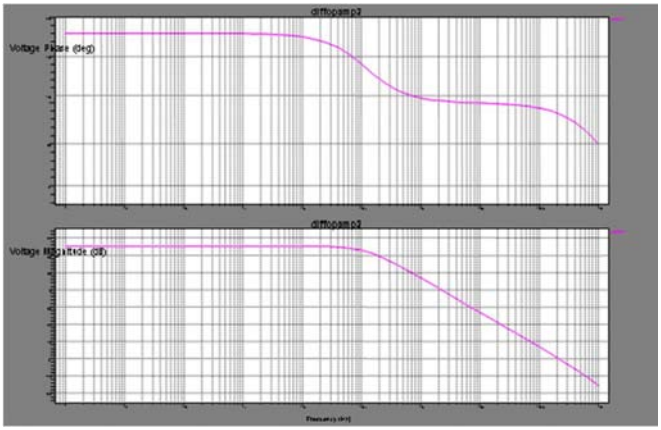

Fig. 10 Gain and phase margin of Op-amp

This arrangement allows the output to be taken at the same bias levels as that of input signal. Even though it is a single stage, the gain is reasonable since the gain is decided by the product of input transconductance and the larger output impedance. The design uses band gap reference and CMFB circuitry. The op-amp results of Fig. 10.Shows a unity gain

frequency of 200MHz at 88° phase margin and a gain of over 70dB and 300 MHz at 72° phase margin for the same gain.

B. Sample and Hold Amplifier

The fully differential Sample and Hold implementation is shown in Fig. 11. We can determine the input/output relationship of sample and hold circuit by evaluating the charge stored on Ci and Cf.
And the expression for output can be written as

$$V_{out} = V_{out+} - V_{out-} = (1+\frac{Ci}{Cf})(V_{in+} - V_{in-}) - \frac{Ci}{Cf}(V_{ci+} - V_{ci-}) \quad (1)$$

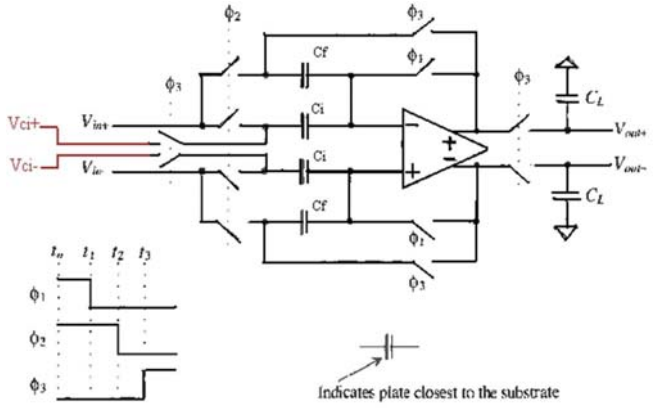

Fig. 11 Switched Capacitor Sample and Hold circuit

If Ci = Cf, then a gain of two is achieved. By connecting Vci+ and Vci- to +Vref and –Vref, we can get 2Vin, (2Vin+Vref) and (2Vin– Vref) required for A/D conversion. The simulated results of Fig. 12 show a sampling rate of 100Msps. The power dissipation is seen to be 8mW for 3.3v supply.

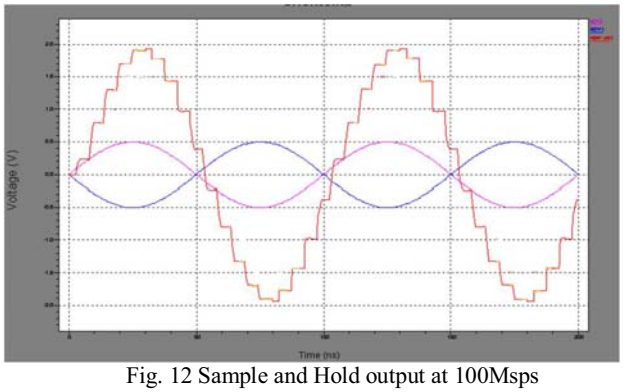

Fig. 12 Sample and Hold output at 100Msps

C. Comparator

The comparator has three stages, the differential stage, decision making stage and the level restoring stage as shown in Fig. 13. The simulation results of Fig. 14 show the comparator delay as 3.28nS.

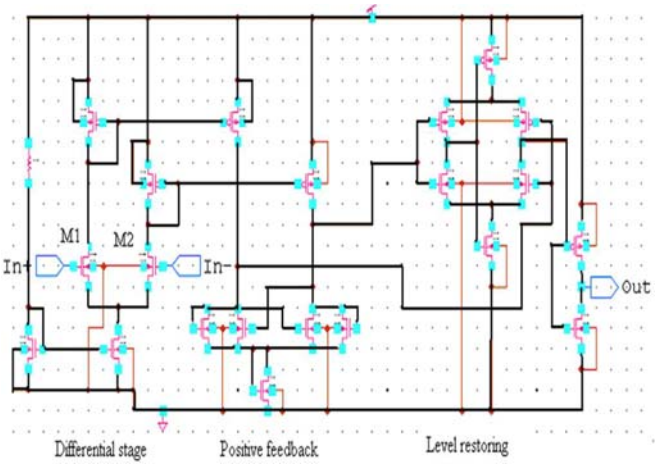

Fig. 13 A High Speed comparator

D.DAC unit

The design uses a simple two way analogue switch for 1 bit DAC and a current steering R-2R ladder DAC for higher number of bits. The resistor string is shared between the flash sub converter and the DAC to minimise the area.

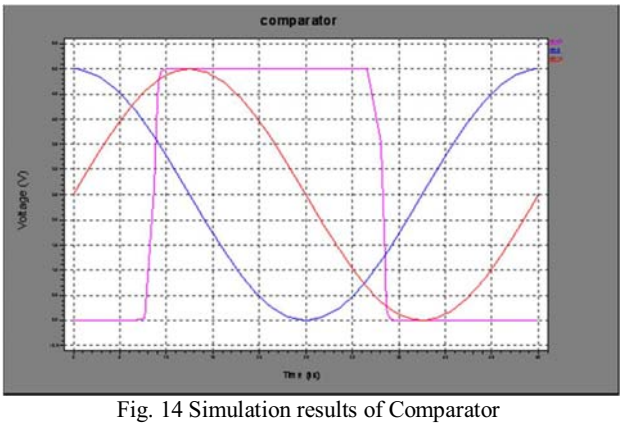

Fig. 14 Simulation results of Comparator

IV. Results

A. Effect of Bits/stage on Area

If the total area of ADC is A_{tot} and area of one stage is A_s, then the total area is given by

$$A_{tot} = (\frac{N-r}{n-r})As \quad (2)$$

Where
N – Number of bits,
n – Number of bits converted per stage and
r – Redundancy.

A_{tot} does not include the area occupied by the digital error correction, bias generation, clock generation and I/O pads. These areas are independent of n. The area of one stage includes the areas of comparator, DAC unit and that of sample & hold.

$$A_s = A_{comp}(2^{N-1}) + A_{DAC} + A_{SH} \quad (3)$$

A_{SH} is observed to be almost proportional to 2^n. As n increases, the numbers of comparators increase and the delay increases. Therefore to reduce the settling time for the given load, the transconductance of the amplifier must be increased proportionally [9]. To increase the transconductance, the area of sample and hold and power dissipation must proportionally increase. If redundancy is introduced, then A_{SH} can be made independent of n (as incomplete settling is allowed). If n is decreased, then number of stages will increase and A_{SH} will increase. Therefore, A_{SH} will dominate for small values of n and if n is large, then A_{comp} dominates over A_{SH}. Fig.16 shows the area distribution of pipelined ADC.

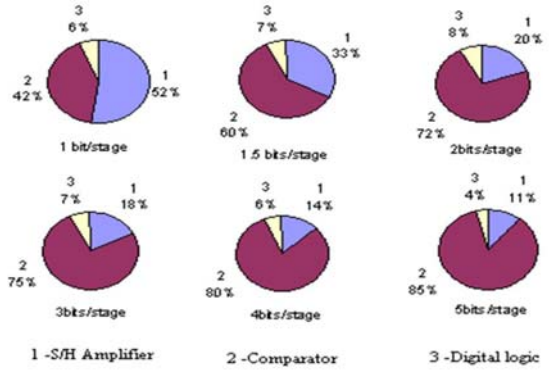

Fig. 15 Area distributions among the blocks

The normalized area as a function of bits/stage is shown in Fig. 16 where we see that the area reduces as we reduce the number of bits /stage showing a dip at 2bits/stage.

B. Effect of Bits/stage on Frequency of conversion

Since the sub ADCs use flash architectures, only two phase clocking is required for conversion. During phase 1, the first stage samples the input while the remaining odd stages samples the residue outputs of even stages. During phase 2, the even stages sample the outputs of odd stages. Therefore, the minimum duration of clock phase is set by the maximum settling time of the Sample and Hold amplifier [10].

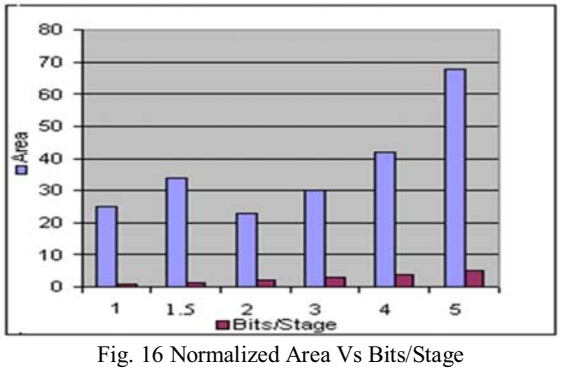

Fig. 16 Normalized Area Vs Bits/Stage

If the two phases are of equal duration, then the maximum frequency of conversion F_c of ADC

$$F_{c\max} \le \frac{1}{2(t_{s\max})} \tag{4}$$

Where t_{smax} is the maximum settling time of Sample and Hold amplifier.

If the Sample and Hold amplifier has a single pole transfer function (dominant pole compensation), and if unity gain frequency is fu, and if the input is a unit step function, then the gain of Sample and Hold amplifier is given by

$$A(t) = 2^{n-r}(1 - e^{-t/\tau}) \tag{5}$$

$$\text{Where } \tau = \frac{2^{n-r}}{f_u} \tag{6}$$

The first term of (5) represents the ideal gain and the second term is because of incomplete settling. Even though Sample and Hold amplifiers are assumed to be identical, their settling times will not be identical and it is observed that the second stage Sample and Hold amplifier has maximum settling time $t_{s\,max}$.

$$t_{s\max} = t_{s2} \approx (N - n + r)2^{n-r}\frac{\ln 2}{f_u} \tag{7}$$

Substituting eq4.5 in eq 4.4 gives

$$F_{c\max} \le \frac{f_u}{(N - n + r)2^{n-r+1}\ln 2} \tag{8}$$

Refer to (8), the maximum frequency of conversion decreases for an increase in the bits/stage. Hence to increase the conversion frequency, the bits/stage must be minimised. The conversion frequency rates for the different bits/stage combinations are shown in Fig. 17.

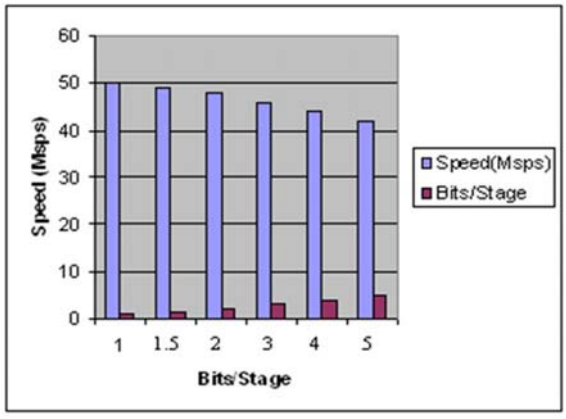

Fig. 17 Frequency Conversion Rates Vs Bits/Stage

C. Effect of Bits/stage On Power dissipation

In ADCs the power is dissipated in Sample and Hold amplifier, sub converter, digital logic and biasing networks. The power dissipated in digital logic and biasing networks is much smaller than that in Sample and Hold amplifiers and sub converters. For reduced bits/stage, power dissipation in Sample and Hold amplifiers dominates while for increased

bits/stage, the sub converter power dissipation dominates over Sample and Hold amplifiers. The power dissipation curves for various bits/stage conversions are shown in Fig. 18.

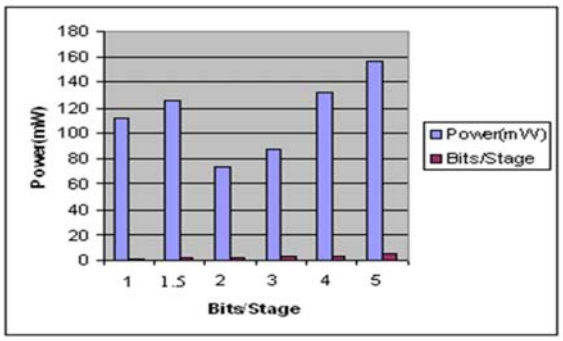

Fig. 18 Power Dissipation Vs Bits/Stage

D. Effect of Bits/stage on Linearity

The error sources in pipelined ADCs are offset, gain and non-linearity errors in Sample and Hold amplifiers, sub converters and DACs. The offset and gain errors can be compensated simply by scaling Rf/Ri or Ci/Cf in the amplifiers and offsetting the input to the ADC. Hence they are not so important in the determination of optimum number of bits/stage conversion. However, the non-linearity error is more difficult to compensate. Fig. 19 shows the signal flow model of a pipelined ADC with n stages and error sources e_1 … e_m …e_n. Here e_m represents the error of stage m and the error includes gain, offset, quantization and non-linearity errors.

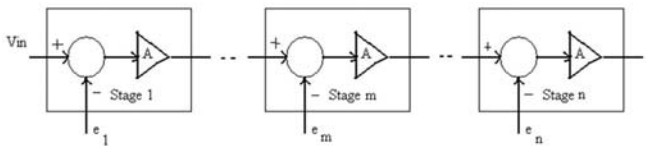

Fig. 19 Signal flow graph model of pipelined ADC

The total error when reflected back into the input can be represented as

$$e_{input} = e1 + \sum_{m=1}^{n-1} \frac{e_{m+1}}{A^m} \tag{9}$$

Equation (9) shows that as gain A increases, the effects of non-idealities of all stages after the first stage becomes smaller. Therefore, to limit the error of ADC to less than ± ½ LSB,

$$e_m \le \frac{FullScaleoutput}{2^{N+1}} A^{m-1} \tag{10}$$

If the error in all stages are identical, i.e. e = e_m , then (9) becomes

$$e_m = e(1 + \sum_{m=1}^{n-1} \frac{1}{A^m}) = e.M \tag{11}$$

Refer to (11) that the total error of all stages is equal to the first stage error multiplied by a factor M, which in turn depends on the gain A of the Sample and Hold amplifier. If A=1 then M = n and if A >> 1then M = 1. The boundary condition between these two cases is with A= 2 gives M=2. Therefore, to make the first stage error to dominate over all other errors, the number of bits/stage must be chosen so that A is >= 2. Hence, more the number of bits/stage less is the non-linearity error in pipelined ADCs. The sub converter and DAC errors can be eliminated by using redundancy and digital error correction mechanism and hence not considered here.

V. Conclusions

With pipelining, the maximum conversion frequency is seen to be almost independent of the number of stages. This allows the bit/stage is to be chosen to fulfil other requirements. This paper concludes that minimizing the bits/stage maximizes the conversion frequency and also minimizes the power dissipation and area requirements and the optimum value is 2bits/stage. The effect of bits/stage on linearity is seen to be small but the linearity is seen to improve if we can increase the number of bits/stage.

Confining the bits/stage to two, we get optimum results with respect to Area, Speed, Power dissipation and linearity.

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