

MULTI VDD (VOLTAGE)

Dynamic power is directly proportional to power supply. Hence naturally reducing power significantly improves the power performance. At the same time gate delay increases due to the decreased threshold voltage. High voltage can be applied to the timing critical path and rest of the chip runs in lower voltage. Overall system performance is maintained. Different blocks having different voltage supplies can be integrated in SoC. This increases power planning complexity in terms of laying down the power rails and power grid structure. Level shifters are necessary to interface between different blocks.

Multiple Voltage ASIC/SoC Design: Classification

Multi voltage design strategies can be broadly classified as follows [1]:

- **Static Voltage Scaling (SVS):** Different but fixed voltage is applied to different blocks or subsystems of the SoC design.
- **Multi-level Voltage Scaling (MVS):** The block or subsystem of the ASIC or SoC design is switched between two or more voltage levels. But for different operating modes limited numbers of discrete voltage levels are supported.
- **Dynamic Voltage and Frequency Scaling (DVFS):** Voltage as well as frequency is dynamically varied as per the different working modes of the design so as to achieve power efficiency. When high speed of operation is required voltage is increased to attain higher speed of operation with the penalty of increased power consumption.
- **Adaptive voltage Scaling (AVS):** Here voltage is controlled using a control loop. This is an extension of DVFS.

Multi Voltage Design Challenges

Level Shifters

Signals crossing from one voltage domain to another voltage domain have to be interfaced through the level shifter buffers which appropriately shift the signal levels. Design of suitable level shifter is a challenging job.

Timing Analysis

Timing analysis of the given design becomes simpler with the single voltage as it can be performed for single performance point based on the characterized libraries. Tools can optimize the design for worst case PVT (Process, Voltage, temperature) conditions. This is not the case with multi voltage designs. Libraries should be characterized for different voltage levels that are used in the design. EDA tool has to optimize individual blocks or subsystems and also multiple voltage domains. This analysis becomes complex for larger ASIC/SoC.

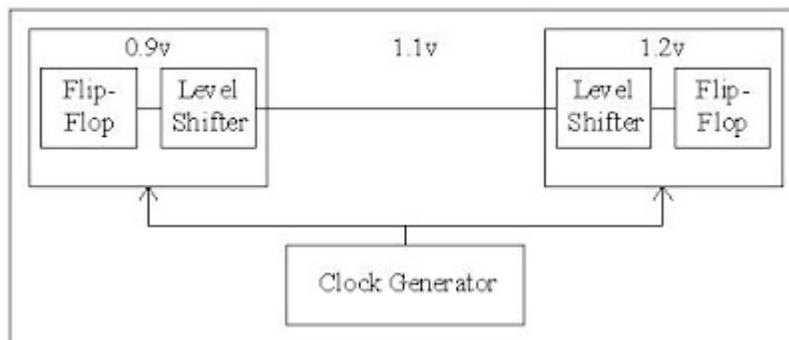
Floor planning and Power Planning

Multiple power domain demands multiple power grid structure and a suitable power distribution among them. For a larger ASIC/SoC more careful floor planning and power planning is essential. The speed in which different power domains switch on or off is also important. A low voltage power domain may activate early compared to the high voltage domain. Multi voltage designs pose additional board level complexities. Separate power supply may necessary to provide different power levels.

Multi Voltage Designs: Timing Issues

Clock

Clock Tree Synthesis (CTS) tools should be aware of different power domains and understand the level shifters to insert them in appropriate places. Clock tree is routed through level shifters to reach different power domains. Simultaneous timing analysis and optimization is necessary for multiple voltage domains. Thus CTS becomes more complex in multi voltage designs.



Timing Issues with multi voltage design

Static Timing Analysis (STA)

Timing analysis for single voltage design is easy. When it comes to static voltage scaling it becomes little tougher job as analysis has to be carried out for different voltages. This methodology requires libraries which are characterized for different voltages used. Multi level and dynamic voltage scaling pose a greater challenge. For each supply voltage level or operating point constraints are specified. There can be different operating modes for different voltages. Constraints need not be same for all modes and voltages. The performance target for each mode can vary. EDA tool should be capable of handling all these situations simultaneously to carry out timing analysis. Different constraints at different modes and voltages have to be satisfied.

Multi Voltage Designs: Power Planning Issues

Efficient power planning is one of the key concerns of modern SoC designs. In multi voltage designs providing power to the different power domains is challenging. Every power domain requires independent local power supply and grid structure and some designs may even have a separate power pad. Separate power pad is possible in flip-chip designs and power pad can be taken out near from the power domain. Other chips have to take out the power pads from the periphery which can put limit to the number of power domains.

Local on chip voltage regulation is good idea to provide multiple voltages to different circuits. Unfortunately most of the digital CMOS technologies are not suitable for the implementation of either switched mode of operation or linear voltage regulations. Separate power rail structure is required for each power domain. These additional power rails introduce different levels of IR drop putting limit to the achievable power efficiency.

Source : <http://asic-soc.blogspot.in/2008/04/multi-vdd-voltage.html>