JUNCTION LEAKAGE AND GIDL

Reverse Biased Diode Current (Junction Leakage)

Parasitic diodes formed between the diffusion region of the transistor and substrate consumes power in the form of reverse bias current which is drawn from the power supply. Junction leakage results from minority carrier diffusion and drift near the edge of depletion regions, and also from generation of electron hole pairs in the depletion regions of reverse-bias junctions. When both n regions and p regions are heavily doped, as is the case for some advanced MOSFETs, there will also be junction leakage due to band-to-band tunneling (BTBT), i.e., electron tunneling from valence band of the p-side to the conduction band of the n-side.

In inverter when input is high NMOS transistor is ON and output voltage is discharged to zero. Now between drain and the n-well a reverse potential difference of Vdd is established which causes diode leakage through the drain junction. The n-well region of the PMOS transistor w.r.to p-type substrate is also reverse biased. This also leads to leakage current at the N-well junction.

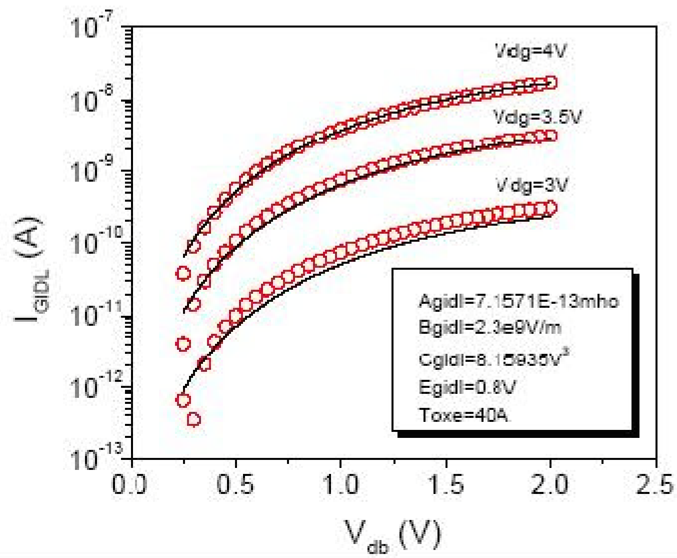
The reverse current can be mathematically expressed [2] as,

$Ireverse=A.Js.(e^{(q.Vbias/kT)}-1)$

where,
Vbias-->reverse bias voltage across the junction
Js-->reverse satuartion current density
A-->junction area

Gate Induced Drain Leakage (GIDL)

Gate-induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. In an NMOS transistor, when the gate is biased to form accumulation layer in the silicon surface under the gate, the silicon surface has almost the same potential as the p-type substrate, and the surface acts like a p region more heavily doped than the substrate. When the gate is at zero or negative voltage and the drain are at the supply voltage level, there can be a dramatic increase of effects like avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate are swept to the substrate, completing the GIDL path. Higher supply voltage and thinner oxide increase GIDL.

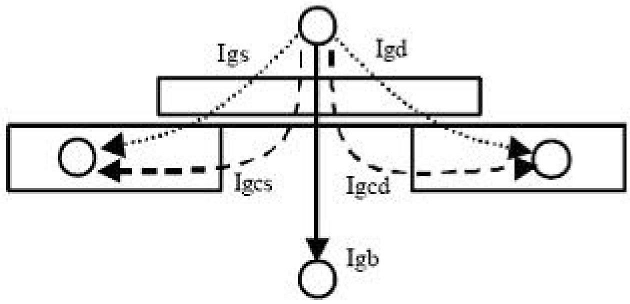


Response of GIDL with varying drain to bulk and gate voltage [1]

Pedram [1] has studied GIDL and has plotted response curve for GIDL with varying drain to bulk and drain to gate voltages as shown in the above figure. From the plot it can be clearly observed that GIDL increases with the increase in V_{db} and V_{dg}.

Gate Oxide Tunneling

When there is a high electric field across a thin gate oxide layer gate oxide tunneling of electrons can result in leakage. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. There can also be direct tunneling through the silicon oxide layer if it is less than 3–4 nm thick. Mechanisms for direct tunneling include electron tunneling in the conduction band (ECB), electron tunneling in the valence band (EVB), and hole tunneling in the valence band (HVB). The dominant source of leakage here is direct tunneling of electrons through gate oxide. This current depends exponentially on the oxide thickness and the V_{DD} [3]



Gate current components flowing between NMOS terminals [3]

Source : http://asic-soc.blogspot.in/2008/04/reverse-biased-diode-current-junction.html