Improving Reliability by Screening

Most of the tests that we deal with in manufacture, such as in-circuit and functional tests, are intended to pick up faults that are ‘active and continuously visible’. Ideally, as part of the production process, we also want to expose faults that are either intermittent or latent in nature. These defects result from many causes, but will become apparent as the normal operational cycle of heating and cooling applies stresses that cause eventual failure. Typical latent and intermittent defects include poor solder joints, defective IC wire bonds, semiconductor impurities, semiconductor defects and component drift.

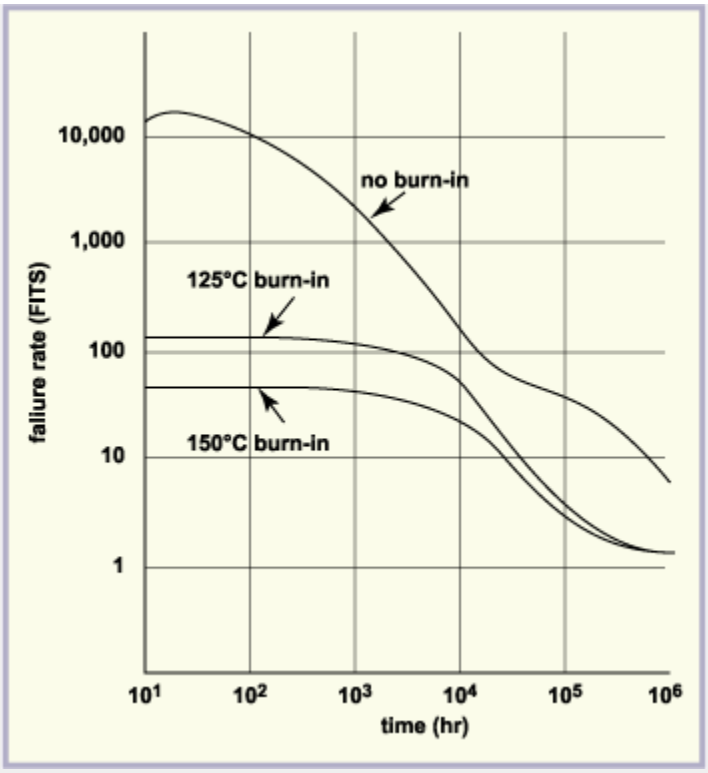
What we need to do is to find some way of applying non-destructive, but still accelerated, tests to production units in order to remove the ‘freak’ failures, and in particular those parts that are likely to fail early in life, yet without reducing the life of good parts.

For components, these accelerated tests are frequently referred to as ‘burn-in’, and this test (described below) is indeed frequently the only stress testing used. However, particularly with more complex assemblies, burn-in may not be the most effective screening procedure, and needs to be supplemented. For example, ‘Thermal Stress Screening’ (TSS) combines burn-in with temperature cycling. Overall, the generic terms ‘process conditioning’, or the more recent ‘Environmental Stress Screening’ (ESS) are to be preferred, since they include the full range of possible tests.

Burn-in

The most basic form of screening regime is to temperature soak the board or component, preferably with power applied, a type of testing called ‘burn-in’, in which the operating temperature of the Unit Under Test (UUT) is raised to a pre-determined level for a specified time, typically for 24–72 hours for assemblies, 4–8 hours for components. The technique has been shown (Figure 1) to enhance the field failure rate of surviving integrated circuits, and there is much other corroborative evidence

Figure 1: IC failure rate vs. system operation time with and without burn-in



after Pollino 1994

Burn-in ovens need careful design to provide:

- an even temperature which is not affected by dissipation in the components
- reliable long-life contacts with the UUTs
- reliable fail-safe power supplies
- automatic removal of failed components from the burn-in circuit
- easy device insertion, extraction and handling.

For these reasons, burn-in equipment is a major expense to purchase, power and maintain, especially for volume manufacturers of components.

The time of component burn-in varies greatly according to the application:

- for commercial users, 4, 6 or 8 hours may be all that is possible, given the volume of production and restrictions on the burn-in capacity available
- for military users, burn-in tests frequently run for a longer period than would be viable for a commercial product and require extended operation at high temperature, which may be beyond the performance limits of polymer encapsulations.

Temperatures used for semiconductors are typically 125°C for plastic-encapsulated parts, and 150°C for discrete hermetic types. Depending on the dissipation of the component, parts may also be exercised at above their working voltage, say 7.5–8V for a 5V logic device.

Although the figure can be much higher for new devices types, burn-in of mature products should be expected only to pull out a small percentage (low single-figure) of failures, typically with oxide, metal migration and step coverage defects rather than assembly problems.

Temperature cycling

Although simple to apply, burn-in does not adequately simulate the operating conditions or apply the levels of stress encountered in the field in severe environments such as automotive applications. Military test engineers discovered that:

- most failures uncovered by burn-in actually occurred during power-up or power-down
- increasing the number of these ‘temperature cycles’ induced significantly more failures than would have occurred in the field
- the more complex a product, the more likely temperature cycling was to expose failures more effectively than burn-in.

The consequent recommendation, to exercise a board assembly by temperature cycling and not just burn-in, is supported by theory, in that mechanical defects

such as cold solder joints or bond wire problems should not be accelerated by burn-in, since only limited mechanical expansion and contraction occurs.

Temperature (or thermal) cycling tests assess performance at varying temperatures, simulating the operating environment. They are intended to assess the integrity of the overall structure of a surface mount assembly and not just individual solder joints, and will reveal problems such as cracking, delamination, joint fatigue failures, seal failures, and internal breaks in tracks and bond wires.

Temperature cycling tests typically use a single test chamber able to change temperature at 3°C per minute. Although faster rates of change apply a higher level of stress and can shorten test times, the energy transfer requirements are considerable, especially when cooling a hot chamber to below –20°C.

Thermal shock testing achieves a much greater rate of temperature change by mechanically moving UUTs from one temperature chamber to another, but this is generally at the expense of higher cost.

When conducting temperature cycling tests the boards are normally always in a powered-up state. Better still is to connect the board to a *slave unit* which drives the board in a fully functional mode, as monitoring performance can uncover intermittent failures, in which a component fails at one temperature, but resumes operation at another.

The actual temperature profile experienced by a large UUT will depend the ability of its surface to dissipate heat, and on the temperature gradients within both the part and the oven. Much depends on chamber and jig design and the velocity and direction of the airflow. In some cases, the test may specify the temperature excursion limits of the UUT, and use chamber temperatures that are hotter and colder than these in order to ensure that the parts reach the correct temperature.

Dwell or soak time does not contribute significantly to product stress, and some users leave chambers at temperature extremes only sufficiently long for the UUTs to reach equilibrium so that functional tests can be carried out.

Typical temperature cycling regimes are 5 or 10 cycles between –40°C to –20°C and +100°C to +125°C, with a rate of temperature change of 3–5°C per minute. For military applications, tests can go down as far as –65°C: it is generally the stresses at *minimum* temperature which cause mechanical failure, whereas *maximum* temperature stresses components, in particular semiconductors and electrolytic capacitors.

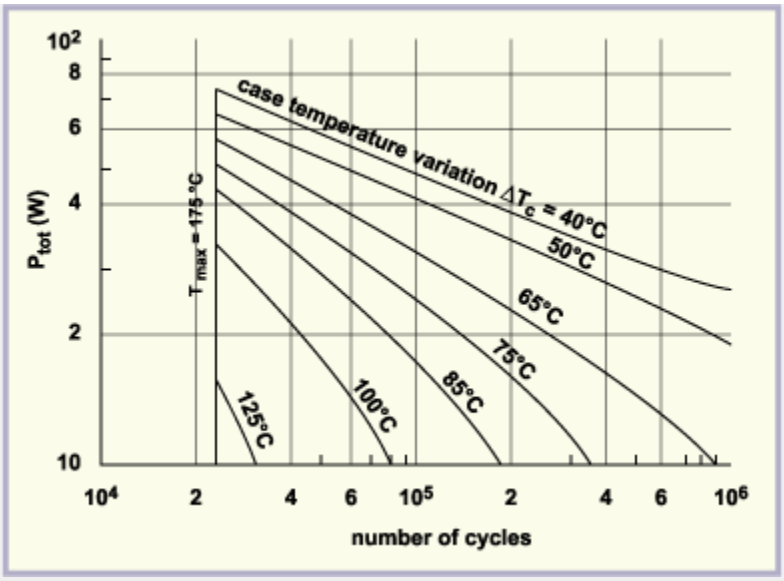
Before specifying the test regimes it is essential to analyse the expected life of the assembly, and from this define the thermal extremes and number of temperature cycles which the product is likely to see over its designed life.

Power cycling

Power cycling, where power is turned on and off at predetermined intervals, is another technique which grew from the observation that most burn-in failures occurred during power-up or power-down, underpinned by the knowledge that CTE mismatch of package materials causes cyclic strain. Power cycling is particularly effective for semiconductors dissipating substantial power, or assemblies with a high power density, and certainly replicates a real-life situation. However, it can be difficult to relate the results of tests under artificial conditions to the expected life of a component in a real operating situation.

Figure 2 is a typical pyramid diagram that links power dissipation, case temperature, and number of cycles to fatigue failure. Using power dissipation speeds up the test and enhances the detection of devices with flaws such as defective die attach, which can then be subjected to more detailed thermal analysis.

Figure 2: Failure due to thermal fatigue as a result of power cycling



Environmental conditioning

As well as extremes of temperature and humidity, electronic parts have to withstand different levels of mechanical shock and vibration, exposure to salt spray, sand, dust, oil or chemicals, depending on application.

A typical **shock test** simulates the stresses resulting from handling, transportation, and operation by applying 5 shock pulses at a selected peak acceleration level for 0.1–0.2ms in each of the 6 possible orientations of a component (relative to its major axis).

This test is for failures due to fracture of the lid seal or lid, or to excessive lid deflection. The direction of mounting is therefore important, since it determines the direction of the stresses in the lid seal and lid, and special mounting fixtures may be required for large multi-chip modules and hybrids.

Three forms of **vibration testing** are used to apply stress to the UUT:

- **Random Vibration** applies band- and amplitude-limited random acceleration over a wide frequency range, usually 10–2,000 Hz.

- **Sine Vibration, Swept Frequency** tests use a swept-frequency or multiple-frequency sinusoidal AC source to detect structural resonances that can cause component failures
- **Sine Vibration, Fixed Frequency** tests use a single-frequency sine wave, usually no higher than 60 Hz.

Each test method requires a 'shaker': mechanical shakers perform fixed-frequency and some swept-frequency tests, but the more common electro-dynamic shakers can be driven by all three types of vibration energy. Depending on the test specification, vibration tests may be carried out on a single axis or three mutually perpendicular axes. Rigid, well-designed fixtures are needed to ensure that the specified stress levels are transmitted to the UUT.

Random-vibration testing is now the preferred method for exposing mechanical design flaws, as it can excite all resonant frequencies throughout the entire test, whereas swept-sine tests do not spend long enough at any one frequency to create sufficient stress. An alternative for less-critical requirements is first to search for significant resonances within the frequency range spectrum of the UUT, and then test for an extended period at each resonant frequency.

For semiconductors in cavity packages, MIL-STD-883 includes **constant acceleration** in its screening tests. This is carried out using a centrifuge at accelerations in the range 5,000g to 300,000g, depending on the package mass. The orientation is such as to accelerate die and bonds away from the package based.

In practice the forces thus applied to aluminium wires are typically two orders of magnitude lower than the pull test break strength, and the test is only effective in breaking bonds with almost zero adhesion or excessive deformation. Because of the higher specific gravity of gold, the test is more severe, and it has been reported that with 50 µm gold wires the elimination of sub-standard parts started between 5,000 and 7,000g, whereas good units survived to 130,000g.

High altitudes, and the accompanying lower atmospheric pressure, exacerbate environmental stress factors. **Low atmospheric pressure** tests simulate high-

altitude conditions, under which systems face reduced heat-transfer efficiency, additional mechanical stress on components with internal cavities, and reduced high-voltage breakdown margins.

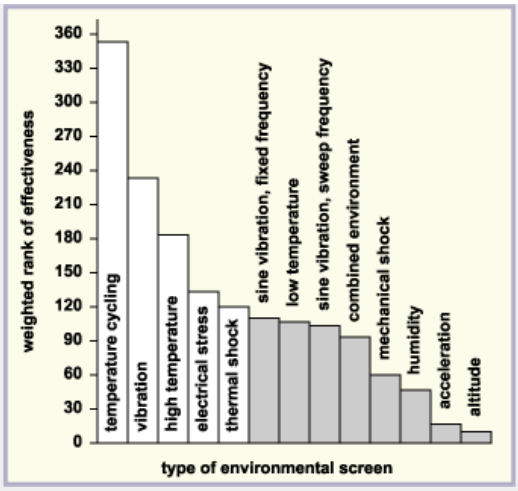
Combining **multiple environmental tests** (such as temperature cycling and altitude) can reduce test times, and some environmental test systems are capable of simulating two or more environments at a time, although this approach is quite expensive.

Multiple tests may also be a requirement when several operational stress factors are present simultaneously. However, before conducting any environmental tests, carefully analyse the product and its specifications to determine whether simultaneous testing is desirable: other research has indicated that it is no more effective than applying the same techniques consecutively.

The effectiveness of screens

The effectiveness of screens varies, the relative value of a test as a means of removing defective parts depending on the application of the module being tested. Figure 3 gives one view of the relative ranking of tests for automotive applications. Gould's selection of temperature cycling, vibration and high temperature life as the 'top three' is probably representative of opinion elsewhere.

Figure 3: Weighted rank of effectiveness of types of environmental screens reveals relative efficiencies



Practical test sequences

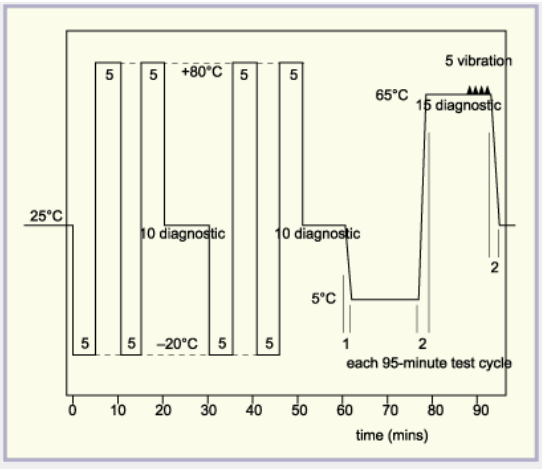
A full set of the tests we have described is expensive, and in consequence its use is restricted to product qualification exercises on mission-critical equipment. However, a suitable selection of tests may be devised to maximise the number of defects discovered at an affordable cost. Such a comprehensive plan, sometimes referred to as Environmental Stress Screening (ESS), is more effective than burn-in in uncovering latent failures.

ESS combines elements such as monitored burn-in, temperature cycling, shock, vibration and other environmental tests, at a severity and in a sequence appropriate for a product's operating environment. ESS programmes can also include power cycling, stabilisation bakes (at low or high temperatures), hermeticity tests, X-ray tests, particle impact noise detection[1], and high-voltage stress. They relate both to complete systems and the components from which they are built.

[1] PIND is a conceptually simple method of detecting loose particles (for example, of solder) sealed within cavity packages and modules by shaking the UUT and using a sensitive microphone to 'listen' for their impact on the walls.

An example of a screening test cycle is diagrammed in Figure 4, and further information on the ESS philosophy is given in the quotation below.

Figure 4: A sample profile for a stress screening experiment



When and why should we screen?

There will be an optimum split of testing between the various stages of inspection and test, depending both on failure mechanisms and rates, and on the stresses which can be applied at any given stage: screening out device failures would take an order of magnitude longer at board level at 85°C than at device level at 150°C.

As with all accelerated testing, there are two key factors:

- matching the test parameters to the defect mechanism
- applying an optimum stress level to force latent defects to fail consistently; whilst staying within the electrical and mechanical limits of the UUT.

Screening is typically applied to semiconductors and modules to be used in military, avionics and other severe environment, high-integrity systems, particularly if a long operating life is required. Probably the best-known of the standards for screening tests is US MIL-STD-883 *Test Methods and Procedures for Microelectronic Devices*, the full text of which (600+ pages!) may be downloaded at Other national and international standards include very similar methods.

MIL-STD-883 and its related specifications suggest a sequence of tests for product conditioning which is well-accepted for military semiconductors, although a small number of good parts will be submitted to destructive testing. It must be emphasised, however, that the screening sequences are generic, and may not be adequate for all applications.

For less severe environments, screening is only justified when:

- the expected proportion defective is sufficiently high that early removal will improve yield in later tests and reliability in service
- the cost of screening is lower than the consequential costs of not screening.

Note that continued improvements in semiconductor device quality have almost eliminated the previous practice of burn-in on receipt by assemblers. In particular, user burn-in of surface mount packages is not advised, as the extra handling involved could lead to damage and degrade the solderability of the contacts. Where required, manufacturers burn-in components as part of their production process.

Some suppliers would advise that it is particularly important to apply such tests to components that are particularly ‘customer sensitive, such as EEPROMs and other memory. In those cases final functional testing is normally carried out after stress testing, although for new designs useful data can be obtained by testing both before and after.

In commercial practice, given that components are now very reliable, screening of assemblies is normally carried out only on a sample basis for design assurance rather than as a production screen, although operational burn-in was formerly quite usual in the manufacture of products such as monitors.

Source : http://www.ami.ac.uk/courses/topics/0188_irbs/index.html