Failure Mechanisms in Other Components

Components in hermetic packages

As explained in *Semiconductor packages*, early active devices needed a hermetic package to prevent junction leakage and degradation of transistor gain caused by moisture and contamination. Nowadays, this approach is more commonly seen in devices such as crystals, where it is important to protect internal surfaces from contamination without making direct contact with them.

'Hermetic' means gas-tight – such packages use ceramic-glass or glass-metal feed-throughs and soldered or welded seals to produce a package whose walls are at least in theory impervious to the outside atmosphere. However, if a package is not properly gas-tight, moisture and contaminants can equally well end up partially sealed in! The consequence is that these packages are usually tested for hermeticity.

Testing involves two stages:

- A 'gross leak' test, for major defects. In the bubble test (or 'dunk test') method most commonly used, the package is immersed in hot liquid and the operator (or automatic equipment) looks for bubbles emerging from the package as the trapped air expands. Typical equipment uses high boiling point perfluorocarbons such as Fluorinert FC-40 and FC-43, held at 125ºC in a back-lit bath with a magnifying front panel. If a large leak is present, a stream of bubbles will be seen rising from the device. This test not only detects a hermeticity failure, but also identifies the location of the leakage site.
- A 'fine leak' test for minor defects. A preliminary is to pressurise the package within a 'bomb' containing an inert tracer gas, usually helium. This forces the tracer gas through any small leaks. Immediately afterwards, the package under test is transferred to a vacuum chamber connected to a 'helium sniffer'. This test can detect leaks of as little as 10^{-8}std.cc/sec^{-11}: for the average package.

[1] *MIL-STD-883 defines a standard leak rate as 'that quantity of dry air at 25ºC in atmosphere cubic centimetres flowing through a leak or multiple leak paths per second when the high pressure side is at one atmosphere and the low side pressure side is at a pressure of not greater than 1mm Hg. Standard leak rate should be expressed in units of atmosphere cubic centimetres per second (atm.cc.s^{-1})'.*

Normal practice is to carry out the tests on sealing after all mechanical tests have been carried out, thus ensuring that handling and any environmental testing has not damaged the integrity of the seal. Because fine-leak testing will expose the package to stress, this is carried out first, followed by the gross leak test.

The fundamental requirement is that the moisture inside the package should not be able to form a layer of surface water which is thick enough to allow sufficient current flow to sustain corrosion. Lau showed this thickness to be 3 molecular layers of condensed or absorbed water. However, it has been calculated that a standard leak rate of 10^{-8} atm.cc.s^{-1} would allow the equivalent of nearly 100,000 layers of water on a chip in ten years, implying that a leak rate of 10^{-13} atm.cc.s^{-1} is really what would be needed to limit the exposure in the same time to safe levels!

Two practical observations must be made about this:

> The MIL-STD-883 requirements are based on what is practicable within a reasonable test schedule, and rely on the fact that hermetic seals are mostly either very much better than the limit or are substantially defective and present definite failures.
>
> This 10^{-13} atm.cc.s^{-1} leak rate is about 10^{-7} times smaller than the lowest permeability observed for polymers – although polymer seals may appear to pass the gas leak-tightness tests, they cannot be regarded as truly hermetic.

A wide range of capacitors and inductors are used within electronic circuits, and all of these can potentially fail. **Film capacitors**, for example, can be damaged by excessive temperature. The materials used being thermoplastics, the problem is less of dielectric failure, leading to short-circuit conditions, as of failure between the external connection and the internal metallising, leading to intermittent or permanent open circuit. Most polymer materials will also absorb moisture, and increased losses can be expected when film capacitors are stored or used in damp environments. Depending on the surface finish, and on the voltage applied, surface tracking and breakdown may also occur.

For **electrolytic capacitors**, the major problems are the application of over-voltage and reverse voltage, about which more will be said later. These are an inevitable consequence of the way in which the dielectric is grown and the counter-electrode made. With time, many larger aluminium electrolytics will also show some adverse effects due to the drying out of the gel dielectric, increasing both ESR and losses.

All types of capacitor will exhibit changes in time and temperature in both insulation resistance and values. Given their initially high values, the former is not usually a problem, but capacitors may well drift out of tolerance, and this can impact on certain types of circuit.

Only NP0 ceramic capacitors should be regarded as sufficiently stable for critical applications, other types exhibiting a continued reduction in value with time. This is related to a change of state which takes plate at the Curie temperature: taken above this temperature, which is typically under the melting point of solder, capacitors with a high dielectric constant reach a maximum and reduce thereafter at a logarithmic rate of 1–2.5% per decade hour. That is, the component will lose 1% of its initial value in the first hour, a further 1% in the next 10 hours and so on. This is in addition to the changes in capacitance that take place over the temperature range.

Film capacitors are generally more stable with time, but may drift if mechanical pressure is applied.

Inductors are relatively stable and reliable, with the exception of parts where the leads are subject to cyclic stresses. However, there may be significant value changes with ferrite-cored components if the ferrite is subjected to shock or other cause of fracture. This is because the fracture creates a break in the magnetic circuit and consequent changes to inductance and mutual inductance. Transformers built with silicon-iron laminations, rather than ferrite cores, also deteriorate with time, although failure is usually gradual, being caused by changes in the insulation between laminates. It is not unusual for both laminated cores and ferrites to become loose and noisy, even if the electrical performance does not deteriorate.

All potted and coated components have potential for failure caused by the absorption of moisture or by temperature cycling (due to the difference in CTE between the materials). The latter problem is particularly severe in constructions such as tantalum capacitors, where some polymer layers are comparatively thick, whilst others are thin. The lack of inherent 'balance' in the structure leads to stresses, which may cause failure.

Other mechanical stresses leading to failure can be the result of the poor mounting of **larger components**. Vibration in particular can cause cyclic component movement which fatigues joints.

Board failures

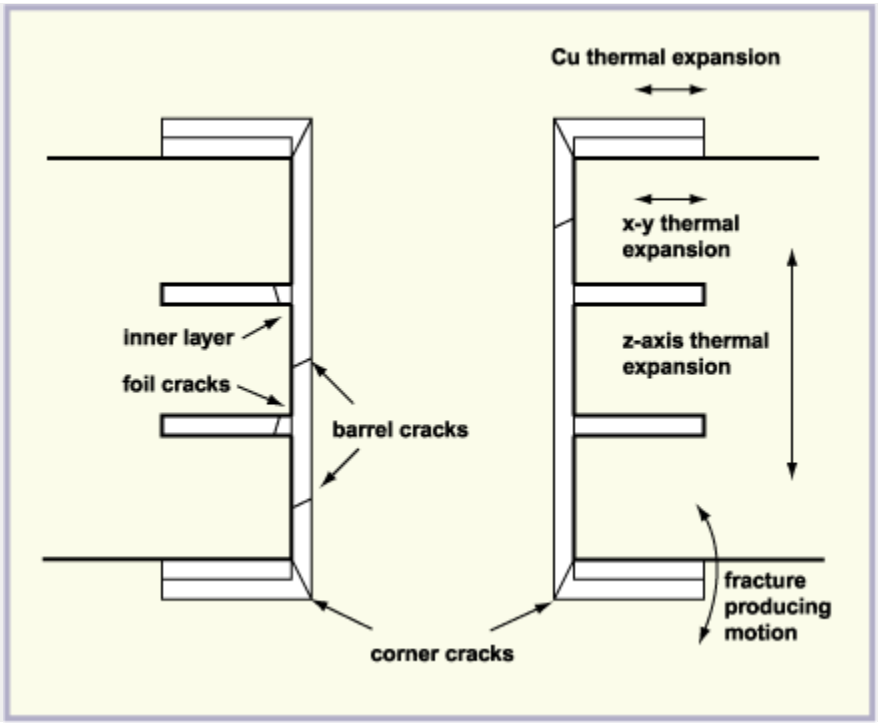
The biggest of the passive components in any assembly is of course the printed circuit board itself. Many of the failures here are related to corrosion, delamination, electromigration and other effects of moisture and will be considered in a later section. There are, however, some other causes for failure during application, as distinct from those problems that are manifest during fabrication and assembly. Chief among these is the result of differences in temperature coefficient between the materials of which the board is made. You will recall that copper has a CTE of around 15 ppm/°C, whereas most resins have substantially higher values in X and Y axes, and higher again in the Z axis, especially once the glass transition temperature has been exceeded.

The most obvious result of differences in CTE is when the board warps. The non-flat surface can give problems during manufacture and result in stresses on components when the board is flattened during assembly, as was indicated earlier in the unit. However, warping is generally a problem that is evident either on receipt of the board or after soldering (especially reflow soldering). Although having long-term reliability implications if stresses are induced because of warping, a warped board is in itself not necessarily unreliable.

However, potential unreliability due to differences in CTE is much more severe when we look at individual holes rather than the complete board. As indicated in Figure 1, there are a number of ways in which the through-hole metallising can

fail. These are conceptually very similar to those experienced with a tubular rivet, and there are many similarities, except of course in scale!

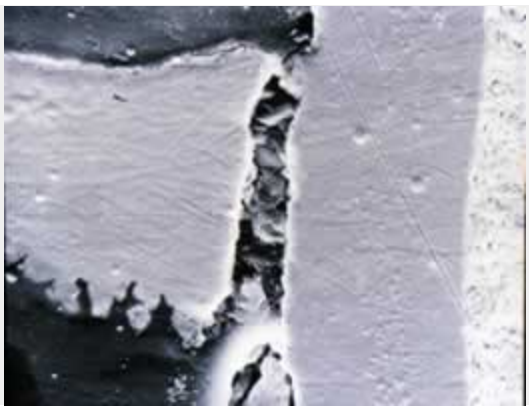
Figure 1: Schematic cross-section of a plated through-hole in a 4-layer PCB showing typical locations of failures due to thermal stress



Illustrated in photographs are typical examples of corner cracking and inner layer cracks. Notice particularly that corner cracking starts from the stress point in the inside, rather than the outside, and can be relatively harmless in appearance. However, given that cracks tend to propagate, intermittencies and open-circuits can be created in a number of places within the through-hole structure.

Cracking on corner of PTH

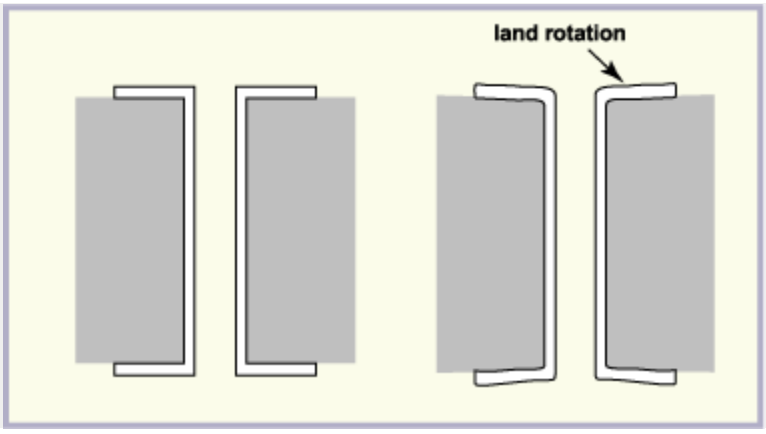
Multi layer junction failure



It is worth noting at this point that a number of these effects are the result of non-elastic behaviour in the materials. As you would expect, when the through-hole is heated, the epoxy expands faster than the copper, setting up a tensile stress in the copper and a compressive stress in the epoxy. In the cooling cycle, the reverse happens, with the epoxy shrinking faster than the copper generating tensile stress in the epoxy and compressive stress in copper.

If the performance of the materials were truly elastic, then there would be no problem. However, after repeated cycling, the epoxy grows, with the result that the board is thicker than in its original condition. This results in what is referred to as the ‘rotation’ of the copper land observed at the outer boundary of the through-hole, as shown in Figure 2.

Figure 2: Effect of thermal ratcheting in PTH structure



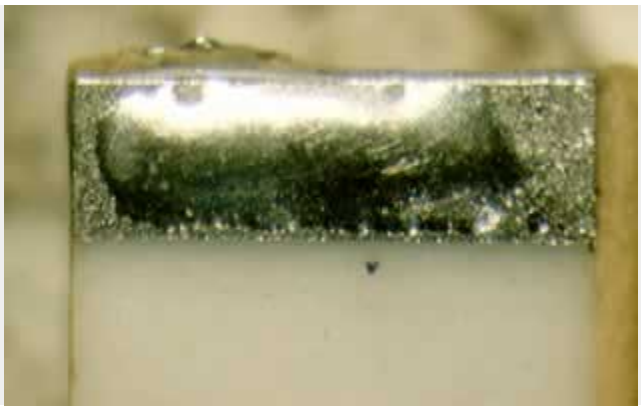
Because the stress exceeds the yield strength of copper, given sufficient temperature cycling, the cumulative strain will cause a crack in the copper barrel. This effect, referred to as ‘ratcheting’ is also seen in solder joints subjected to cyclical stresses.

Also important for long term life is the survival of solder joints. As with the plated through-hole, failures here need some understanding of the metallurgical considerations, and this is a separate topic at the end of this unit.

Solderability degradation

As discussed in other units, many apparent component failures are really failures to make an adequate solder joint. Both the surface finish of a component and the conditions under which it is stored may affect the wettability of the component and hence its fitness for purpose in the assembly. As was explained in *How joints are made* and *Selecting a board finish*, board and component solderability is extremely variable and damp and heat combined will do much to reduce the wettability of even the more robust surface.

Ceramic capacitor termination showing poor solderability



Source: http://www.ami.ac.uk/courses/topics/0141_fmoc/index.html