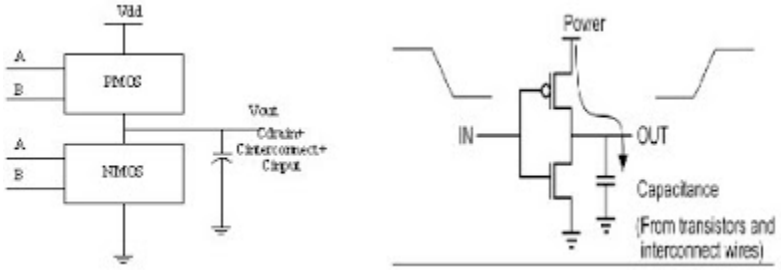
DYNAMIC POWER

As the name indicates it occurs when signals which go through the CMOS circuits change their logic state. At this moment energy is drawn from the power supply to charge up the output node capacitance. Charging up of the output capacitance causes transition from 0V to Vdd. Considering an inverter example power drawn from the power supply is dissipated as heat in pMOS transistor. On the other hand charge down process causes NMOS transistor to dissipate heat.

Output capacitance of the CMOS logic gate consists of below components:

1) **Output node capacitance of the logic gate:** This is due to the drain diffusion region.
2) **Total interconnects capacitance:** This has higher effect as technology node shrinks.
3) **Input node capacitance of the driven gate:** This is due to the gate oxide capacitance.



Dynamic power dissipation in CMOS inverter [1]

The average power dissipation of the CMOS logic circuit can be mathematically expressed [2]. Integrating the instantaneous power over the period of interest, the energy E_{VDD} taken from the supply during the transition is given by

$E_{VDD}= 0->\infty\int I.\ V_{DD}(t).V_{DD}.dt$

$=V_{DD}.\ 0->\infty\int C_L.(dvout/dt).dt$

$= C_L.V_{DD}.\ 0->V_{DD}\int.dvout$

$= C_L.V_{DD}^2$

Similarly integrating the instantaneous power over the period of interest, the energy Ec stored in the capacitor at the end of transition is given by,

Ec = $0->\infty \int I.V_{DD}(t).Vout.dt$

$= 0->\infty \int C_L.(dvout/dt).vout.dt$

$= C_L.$(integration from 0 to VDD).Vout.dvout

$= (C_L.V_{DD}^2)/2$

Therefore energy stored in capacitor is= $C_L.V_{DD}^2 / 2$.

This implies that half of the energy supplied by the power source is stored in C_L. The other half has been dissipated by the PMOS devices. This energy dissipation is independent of the size of the PMOS device. During the discharge phase the charge is removed from the capacitor, and its energy is dissipated in the NMOS device.

Each switching cycle takes a fixed amount of energy = $C_L. V_{DD}^2$.

If a gate is switched on and off ‘fn’ times / second, then Pdynamic = $C_L. V_{DD}^2. fn$.

Where fn ✳ frequency of energy consuming transitions. This is also called "switching activity".

In general we can write,

Pdynamic = $Ceff.V_{DD}^2.f$

Where f ✳ maximum switching activity possible i.e. clock rate.

Hence,

$P_{avg}= 1/T [0->T/2\int Vout (-C_{load}.dVout/dt)dt+T/2->T\int(V_{DD}-Vout)(C_{load}.dVout/dt) dt]$

i.e. $P_{avg}=1/T\ C_{load}.V_{DD}^2$
i.e. $P_{avg}=C_{load}.V_{DD}^2.F_{clk}$

Here energy required to charge up the output node to Vdd and charge down the total output load capacitance to ground level is integrated. Applied input periodic waveform having its period T is assumed to be having zero rise and fall time. Note that average power is independent of transistor size and characteristics.

Internal power

This is the power consumed by the cell when an input changes, but output does not change [3]. In logic gates not every change of the current running through an input cell necessarily leads to a change in the state of the output net. Also internal node voltage swing can be only Vi which can be smaller than the full voltage swing of Vdd leading to the partial voltage swing.

Below mentioned steps can be taken to reduce dynamic power

1) Reduce power supply voltage Vdd
2) Reduce voltage swing in all nodes
3) Reduce the switching probability (transition factor)
4) Reduce load capacitance

Source : http://asic-soc.blogspot.in/search/label/Dynamic%20Power