

Module

3

DC to DC Converters

Lesson 24

CuK and Sepic Converter

Instructional objective

On completion the student will be able to

- Compare the advantages and disadvantages of $\hat{C}uK$ and Sepic converters with those of three basic converters.
- Draw the circuit diagrams and identify the operating modes of $\hat{C}uK$ and Sepic converters.
- Draw the waveforms of the circuit variables associated with $\hat{C}uK$ and Sepic converters.
- Calculate the capacitor voltage ripples and inductor current ripples in $\hat{C}uK$ converter.

24.1 Introduction

Switch Mode Power Supply topologies follow a set of rules. A very large number of converters have been proposed, which however can be seen to be minor variations of a group of basic DC-DC converters – built on a set of rules. Many consider the basic group to consist of the three: BUCK, BOOST and BUCK-BOOST converters. The CUK, essentially a BOOST-BUCK converter, may not be considered as basic converter along with its variations: the SEPIC and the zeta converters.

The Canonical Cell forms the basis of analyzing switching circuits, but the energy transport mechanism forms the foundation of the building blocks of such converters. The Buck converter may consequently be seen as a Voltage to Current converter, the Boost as a Current to Voltage converter, the Buck-Boost as a Voltage-Current-Voltage and the CUK as a Current-Voltage-Current converter. All other switching converter MUST fall into one of these configurations if it does not increase the switching stages further for example into a V-I-V-I converter which is difficult to realize through a single controlled switch. It does not require an explanation that a current source must be made to deliver its energy into a voltage *sink* and vice-versa. A voltage source cannot discharge into a voltage sink and neither can a current source discharge into a current sink. The first would cause current stresses while the latter results in voltage surges. This rule is analogous to the energy exchange between a *source* of Potential Energy (Voltage of a Capacitor) and a *sink* of Kinetic Energy (Current in an Inductor) and vice-versa. Both can however discharge into a dissipative load, without causing any voltage or current amplification. The resonant converters also have to agree to some of these basic rules.

24.2 Analysis of \hat{C} uK converter

The advantages and disadvantages of three basic non-isolated converters can be summarised as given below.

- (i) Buck converter

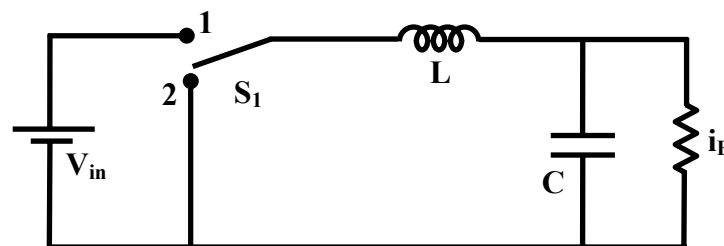


Fig. 24.1: Circuit schematic of a buck converter

Features of a buck converter are

- Pulsed input current, requires input filter.
- Continuous output current results in lower output voltage ripple.
- Output voltage is always less than input voltage.

(ii) Boost converter

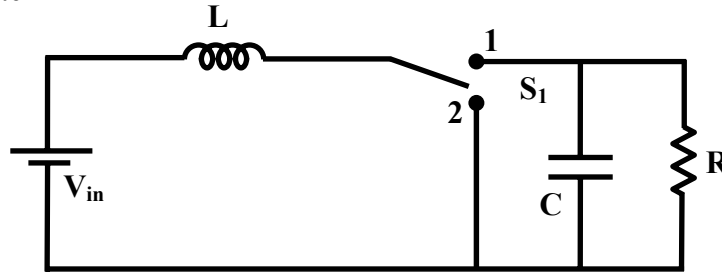


Fig. 24.2: Circuit schematic of a boost converter

Features of a boost converter are

- Continuous input current, eliminates input filter.
- Pulsed output current increases output voltage ripple.
- Output voltage is always greater than input voltage.

(iii) Buck - Boost converter

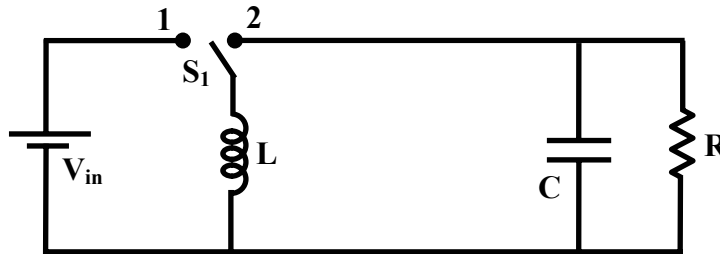


Fig. 24.3: Circuit schematic of a buck boost converter

Features of a buck - boost converter are

- Pulsed input current, requires input filter.
- Pulsed output current increases output voltage ripple
- Output voltage can be either greater or smaller than input voltage.

It will be desirable to combine the advantages of these basic converters into one converter.

$\hat{C}uK$ converter is one such converter. It has the following advantages.

- Continuous input current.
- Continuous output current.
- Output voltage can be either greater or less than input voltage.

$\hat{C}uK$ converter is actually the cascade combination of a boost and a buck converter.

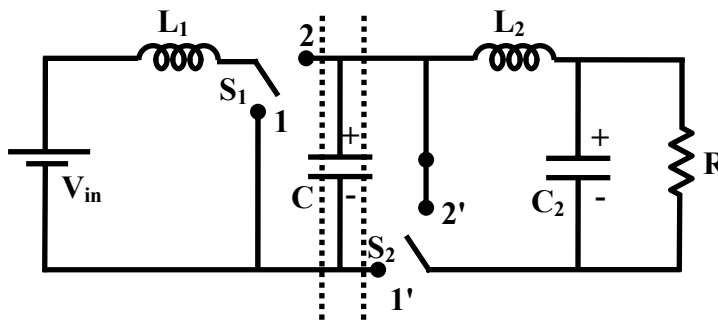


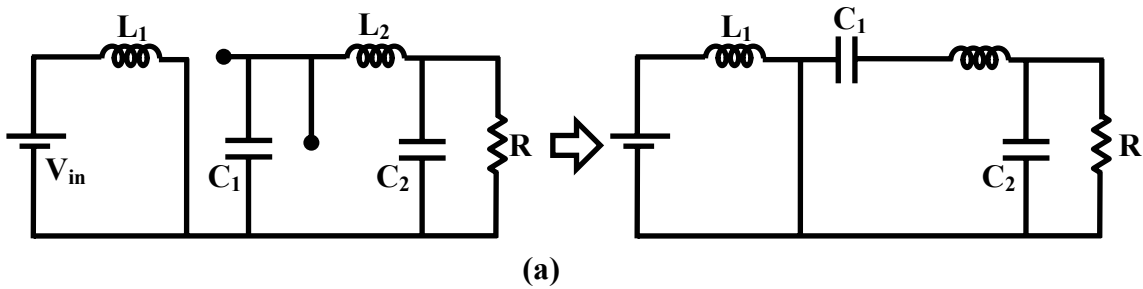
Fig. 24.4: Circuit schematic of a boost-buck converter

S_1 and S_2 operate synchronously with same duty ratio. Therefore there are only two switching states.

(i) $0 < t \leq DT$
 S_1 to (1)

& S_2 to (1')

The circuit configuration is given below



(ii) $DT < t < T$; S_1 to (2) & S_2 to (2')

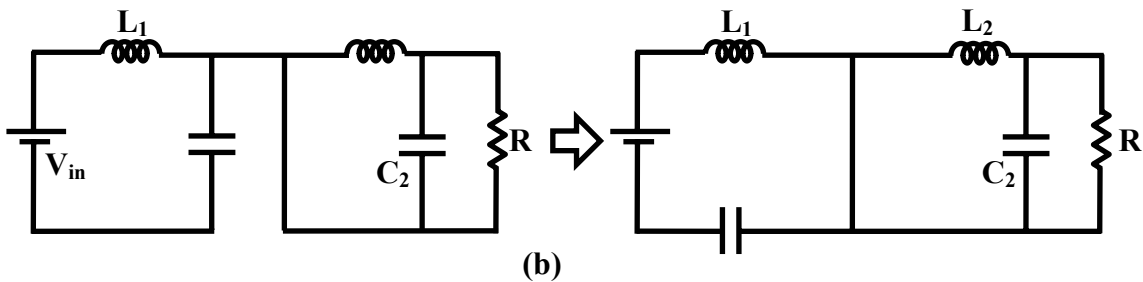


Fig. 24.5: Circuit topology of a boost-buck converter during different switching intervals

(a) $0 \leq t < DT$, (b) $DT \leq t < T$

These two topologies can also be obtained from the following circuit which is the so called $\hat{C}uK$ converter.

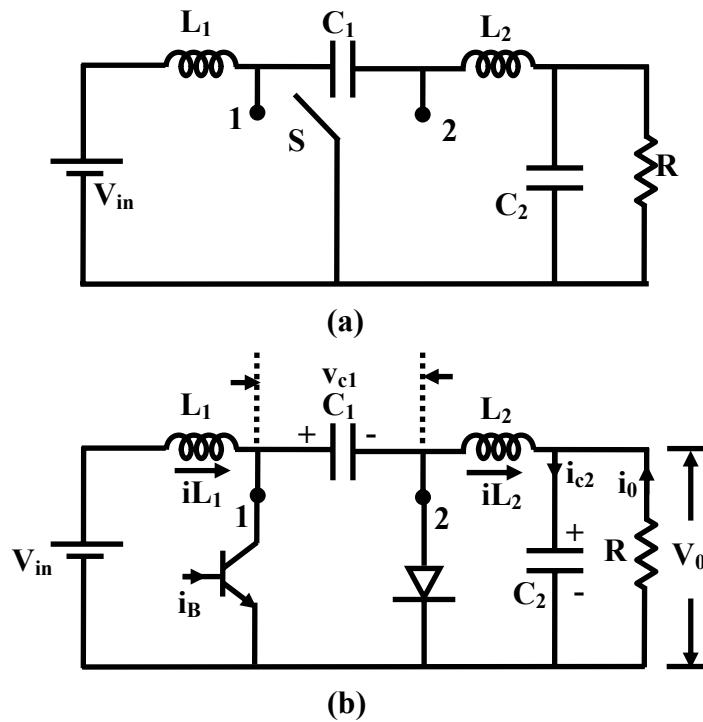


Fig. 24.6: Schematic and Circuit representation of ĈuK converter.
 (a) Schematic diagram, (b) Circuit diagram

24.2.1 Expression for average output voltage and inductor currents

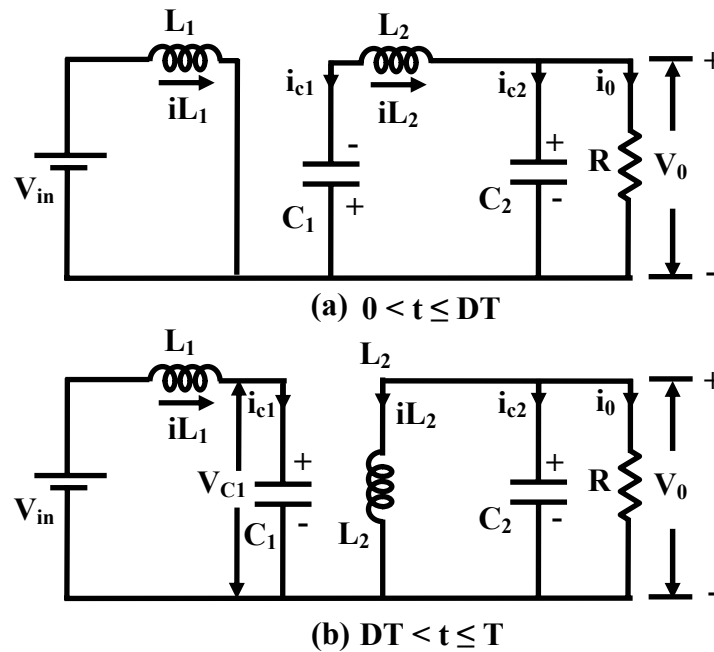


Fig. 24.7: Equivalent Circuit of a ĈuK converter during different conduction modes.
 (a) $0 < t \leq DT$ (b) $DT < t \leq T$

Applying Volt-sec balance across L_1

$$V_{in}DT + (V_{in} - V_{C1})(1-D)T = 0 \quad (24.1)$$

$$\therefore V_{in}(1-D)V_{C1} = 0$$

$$\text{or } V_{C1} = \frac{V_{in}}{1-D} \quad (24.2)$$

Applying Volt-sec balance across L_2

$$(V_0 + V_{C1})DT + V_0(1-D)T = 0 \quad (24.3)$$

$$\text{or } V_0 + DV_{C1} = 0 \quad (24.4)$$

$$\text{or } V_0 = -DV_{C1} = -\frac{DV_{in}}{1-D} \quad (24.5)$$

Expression for average inductor current can be obtained from charge balance of C_2

$$I_{L2} + I_0 = 0 \quad (24.6)$$

$$\therefore I_{L2} = -I_0 = -\frac{V_0}{R} = \frac{D}{1-D} \frac{V_{in}}{R} \quad (24.7)$$

From power balance

$$V_{in}I_{L1} = V_0I_0 = \frac{V_0^2}{R} = \frac{D^2}{(1-D)^2} \frac{V_{in}^2}{R} \quad (24.8)$$

$$\therefore I_{L1} = \frac{D^2}{(1-D)^2} \frac{V_{in}}{R} \quad (24.9)$$

24.2.2 Current ripple and voltage ripple calculations

The waveforms of different circuit variables of Fig. 24.7 are given in Fig. 24.8.

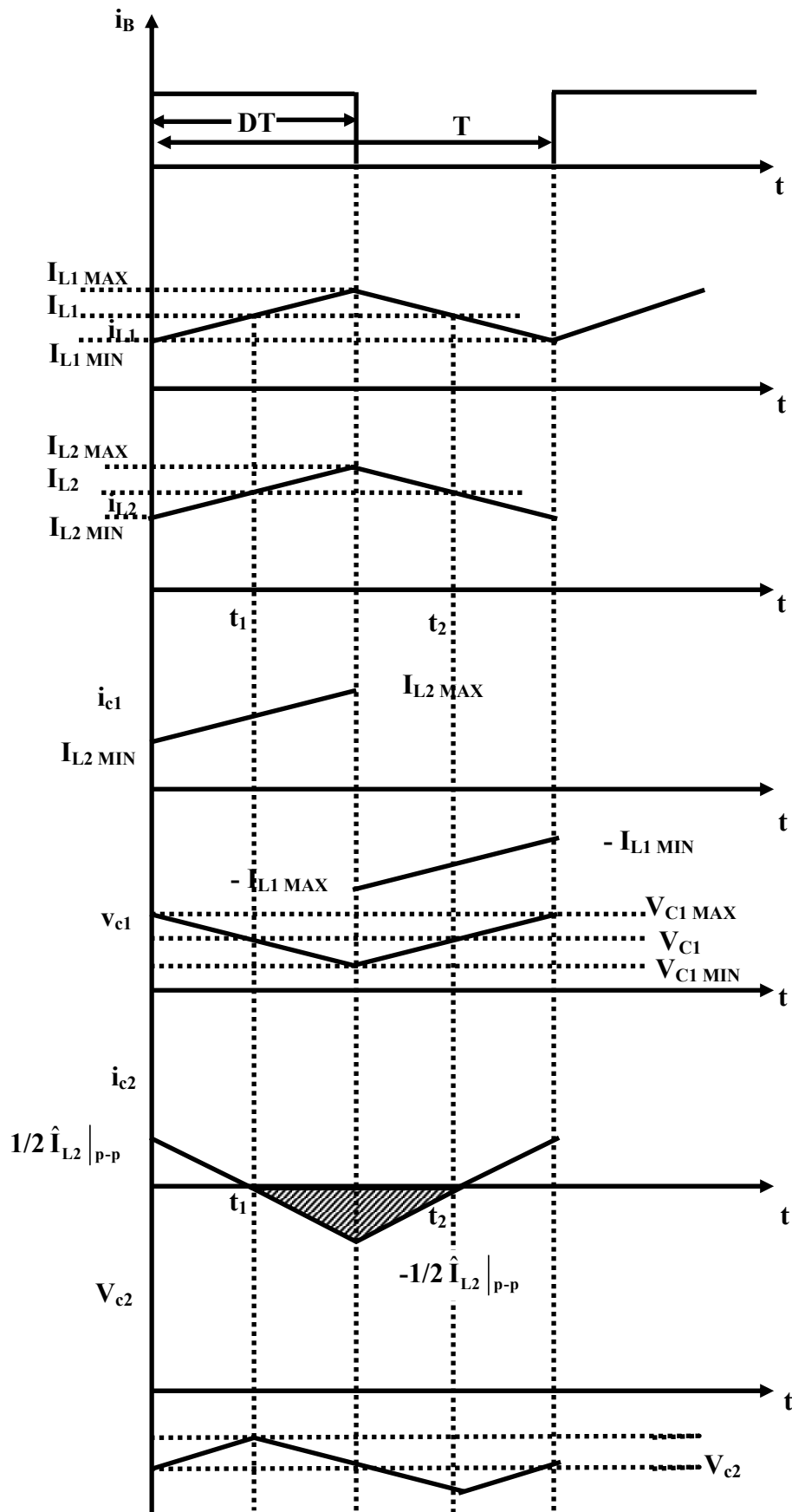


Fig. 24.8: Waveforms of circuit variables in a ĈuK converter.

From the waveforms of Fig. 24.8

$$I_{L1MAX} = I_{L1MIN} + \frac{DV_{in}T}{L_1} \quad (24.10)$$

$$\hat{I}_{L1}\Big|_{p-p} = I_{L1MAX} - I_{L1MIN} = \frac{V_{in}DT}{L_1} \quad (24.11)$$

From equation 24.9

$$I_{L1MAX} + I_{L1MIN} = 2I_{L1} = \frac{2D^2}{(1-D)^2} \frac{V_{in}}{R} \quad (24.12)$$

$$\therefore I_{L1MAX} = \left[\frac{D}{(1-D)^2} + \frac{RT}{2L_1} \right] \frac{DV_{in}}{R} \quad (24.13)$$

$$I_{L1MIN} = \left[\frac{D}{(1-D)^2} - \frac{RT}{2L_1} \right] \frac{DV_{in}}{R} \quad (24.14)$$

$$I_{L2MAX} = I_{L2MIN} - \frac{V_0}{L_2}(1-D)T = I_{L2MIN} + \frac{V_{in}}{L_2}DT \quad (24.15)$$

$$\therefore \hat{I}_{L2}\Big|_{p-p} = I_{L2MAX} - I_{L2MIN} = \frac{V_{in}DT}{L_2} \quad (24.16)$$

From equation 24.7

$$I_{L2MAX} + I_{L2MIN} = -2I_0 = \frac{2D}{1-D} \frac{V_{in}}{R} \quad (24.17)$$

$$\therefore I_{L2MAX} = \left[\frac{1}{1-D} + \frac{RT}{2L_2} \right] \frac{DV_{in}}{R} \quad (24.18)$$

$$I_{L2MIN} = \left[\frac{1}{1-D} - \frac{RT}{2L_2} \right] \frac{DV_{in}}{R} \quad (24.19)$$

For calculating voltage ripples it is noted that

$$v_{c1} = \frac{1}{C1} \int_0^{DT} i_{c1} dt \quad (24.20)$$

$$\text{but for } 0 < t \leq DT \quad i_{c1} = i_{L2} \quad (24.21)$$

$$\frac{1}{C1} \int_0^{DT} i_{c1} dt = \frac{1}{C1} \int_0^{DT} i_{L2} dt \quad (24.22)$$

$$\text{or } \hat{v}_{c1} = \frac{DT}{C1} \left[\frac{I_{L2MAX} + I_{L2MIN}}{2} + \frac{RT}{2L_2} \right] = \frac{DTI_{L2}}{c1} = \frac{I_0DT}{c1} \quad (24.23)$$

$$\text{or } \hat{v}_{c1} = \frac{D^2V_{in}T}{RC1(1-D)} \quad (24.24)$$

$\hat{v}_{c2} = \left| \frac{1}{c2} \int_{t1}^{t2} i_{c2} dt \right|$ which is the hatched area under i_{c2} waveform in Fig. 24.8

$$\therefore \hat{v}_c = \frac{1}{c1} \times \frac{1}{2} \times \frac{T}{2} \times \frac{V_{in}DT}{2L_2} = \frac{V_{in}DT^2}{8L_2C_2} \quad (24.25)$$

Equations 24.11, 24.16, 24.24 and 24.25 can be utilized to design a $\hat{C}uK$ converter of given specification

The SEPIC Converter

The previous chapter discussed the single stage conversion Buck and Boost converters along with the two-stage Buck-Boost converter. This chapter offers a few additional topologies.

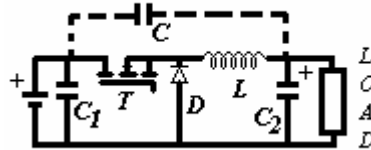


Fig. 24.9(a): A basic converter: BUCK converter

Fig. 24.9(a) is that of a basic Buck converter. From the voltage source C_1 , the converter charges the current sink constituted by the inductor-diode (L-D). The current is further converted into voltage without a switching stage (amplification) at C_2 . The canonical switching cell is approached if the capacitors C_1 and C_2 are combined to be represented by a single capacitor C . The cell includes T-C-L-D, the basic building block of DC-DC converters. The Boost converter is realized if the positions of D and T are interchanged in Fig.24.9 (a). Now power flows in from the right. Here, the energy stored in the inductor during each ON period of switch T is transferred to the Capacitor during its OFF period.

The CUK converter as the dual of the Buck-Boost converter has current input and current output stages. The basic SEPIC is a modification of the basic Boost and the CuK topologies. Consider the Boost converter in Fig 24.9(b). At steady state, the average voltage across the input inductor is zero. Equating the inductor voltages for the period when the switch T is ON with that when it is OFF,

$$V_{in} \cdot T_{ON} = (V_{out} - V_{in}) \cdot T_{OFF} \quad (24.26)$$

$$\text{or, } V_{out} = \left(\frac{1}{1-\delta}\right) \cdot V_{in}$$

where, δ is the duty ratio of the switch.

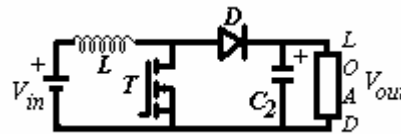


Fig. 24.9(b): BOOST converter

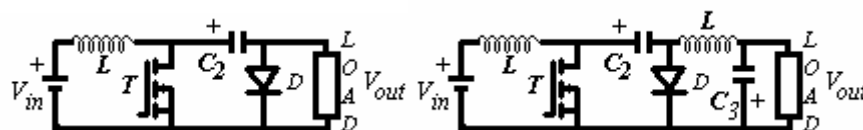


Fig. 24.10 Modified Boost with load across Diode for Boost-Buck Operation. (left) without output filter, (right) with filter.

In the path, V_{in} -L-D- V_{out} , in Fig. 24.9(b), the average voltages across all the elements are known. Thus, that appearing across the diode D is $V_{out} - V_{in}$. This voltage from Eqn 1 is:

$$V_D = [(1/1 - \partial) - 1] \cdot V_{in}$$

$$= (\partial / (1 - \partial)) V_{in}$$

A Boost-Buck converter is thus realized. This is the voltage that would appear in an unfiltered form at the load in Fig. 24.10 (left). Now, since the source is a current source, the output stage must be capacitive (voltage sink) which is taken care of by C_2 -D. The voltage across D has high ripples, which can be filtered much like the Buck converter with an L (and a C_3). The CUK converter is thus realized. It is a I-V-I converter.

A glaring drawback of this derived converter topology is that the polarity of the output is reversed. This is not acceptable for various reasons.

Now it is the turn of the Diode to be interchanged with the filter inductor. The inductor is thus converted to be part of the switching circuit and it not just a filter. The SEPIC results – not an entirely different one - but easily derivable from the previous topologies.

The SEPIC officially stands for “Single-Ended Primary Inductance Converter”. However, the unofficial interpretation is more descriptive: “Secondary Polarity Inverted Cuk”.

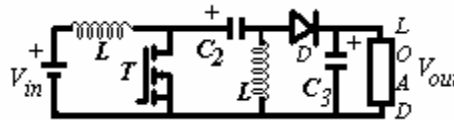


Fig. 24.11(a): The basic SEPIC topology

Again, the basic input–output relation can be derived by considering the two inductors to have average null voltage across themselves.

If the link capacitor has a voltage V_c across itself (consider it to be reasonably constant), then for the input inductor, the volt-secs during the ON and OFF periods of the switch are:

$$V_{in} \cdot T_{ON} = (V_c - V_{out} - V_{in}) T_{OFF}$$

or,
$$V_c = V_{out} - V_{in} \left(\frac{1}{T_{OFF}} \right)$$
 (24.27)

For the output inductor,

$$V_c \cdot T_{ON} = V_{out} \cdot T_{OFF}$$
 (24.28)

Eliminating, V_c and writing $T_{ON} = \partial \cdot T$,

$$V_{out} = (\partial / (1 - \partial)) V_{in}$$
 (24.29)

Thus the SEPIC is also basically a BOOST-BUCK converter akin to the CUK converter. (The Boost stage comes first followed by the Buck stage and it is also I-V-I converter)

In the practical SEPIC converter, the two inductors are coupled with the polarities as indicated by dots in Fig. 24.11(a). The turns ratio is and the coupling is very tight. For such a coupled-transformer SEPIC, equating the positive and negative volt-secs for the two inductors,

$$(V_{in} \cdot K \cdot V_c) \cdot T_{ON} = (V_{out} + V_c - V_{in} - K \cdot V_{out}) \cdot T_{OFF}$$
 (24.30)

for the input inductor, and

$$(V_C - K' V_{in}) T_{ON} = [V_{out} - K'(V_{out} + V_C - V_{in})] T_{OFF} \quad (24.31)$$

Equations (24.28) and (24.29) can be obtained from the above two by substituting both K and K' to zero to have no coupling between the two coils.

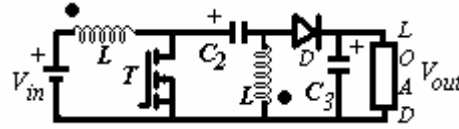


Fig. 24.11(b) The practical SEPIC topology with coupled inductors

The above two equations result in an identity to indicate that such a system cannot work.

This can be explained by examining the operation of the circuit. Initially when the transistor is OFF, the capacitor C_2 charges to the supply voltage V_{in} . When the transistor is switched ON, the resulting active circuit is shown in Fig 24.12.

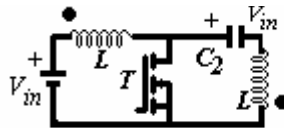


Fig. 24.12: Active part of the circuit when transistor is switched with C_2 charged to V_{in}

The circuits to the left and right of the transistor are identical and both the windings are induced with the supply voltages, resulting in null emfs on either side, which explains why the ideal circuit will not work. However, neither the coupling between the inductors nor the effective turns ratio can be unity. This results in a circuit with the features of the uncoupled circuit and the circuit performs.

The second voltage source, V_C , induces $N.V_C$ into the primary, where N is the turns ratio. For the interesting case, $V_{in} = V_C = V_I$, if the turns ratio, n , is increased slightly from unity, by $1/k$ (where $k < 1$ is the coupling coefficient between windings), then the voltage induced by V_{in} will increase the voltage at the Drain of the transistor to $N.V_I$, thereby "bootstrapping" the leakage inductance of the input inductor. Because the voltage at each end of this leakage inductance is the same, its inductance is effectively infinite. Consequently, all variations in magnetizing current, (through M) due to a varying V_I is supplied from the secondary winding source. By symmetry, setting $n = k$ causes the secondary-winding current to become constant while the primary source supplies the magnetizing-current variations.

This effect can be desirable because, for $n = 1/k$, it results in constant (DC) primary current. Noisy switching current does not appear at the converter input but is diverted instead to the secondary winding. However, typical values of k are slightly less than one, and turns ratios of nearly 1:1 may not be easy to wind. One simplification is to use a 1:1 transformer, such as a low-cost, commodity, common-mode power-line input-filter choke, and add a small additional inductance in series with the primary winding. This effectively increases the leakage inductance so that the same secondary-winding dominance of magnetizing current is obtained with $n = 1$.

The circuit is an alternative to the Boost converter and outputs an range which includes the input range also being a Boost-Buck converter. It is superior to the other converters both in terms of the input current purity and efficiency.

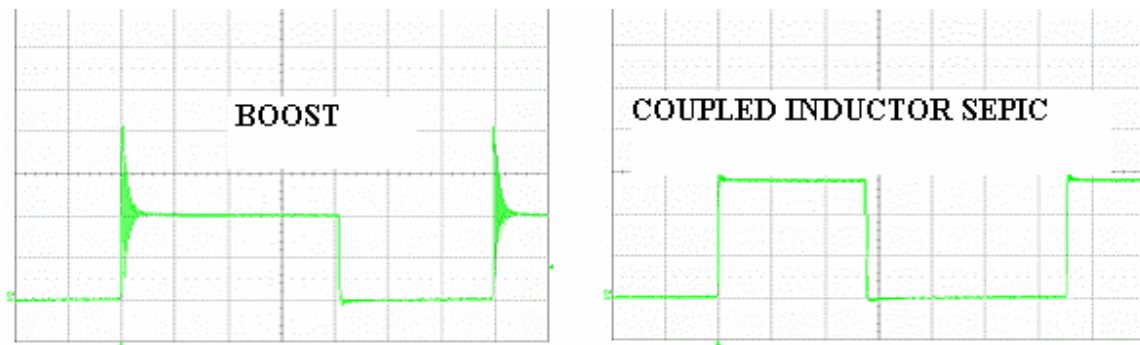


Fig. 24.13: Drain voltages of FLYBACK and SEPIC converters

The waveforms in Fig. 24.13 show the voltage at the transistor Drain present on the fly back (Boost) and SEPIC circuits. The fly back transformer leakage inductance produces a voltage spike that adds an additional level to the "flat-top" voltage. This level is about 1.5 times the supply voltage for inputs around 20 V. In comparison, the SEPIC FET switching waveform is clamped, and shows very little overshoot, or ringing. This clamping results in less switching-loss, output voltage noise and a power stage that can be operated at a much higher frequency than that of the fly back.

Again, the fly back transformer leakage inductance also produces a significant voltage spike relative to the SEPIC at the output diode. A relatively high voltage (~200V) output diode is required for the fly back to handle the large negative ringing compared to the SEPIC's 60V Schottky diode. The 0.5 volt forward drop of the SEPIC's Schottky diode relative to the one volt forward drop of the flyback's ultra-fast diode, results in significant power savings for the SEPIC.

Source:

[http://www.nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Power%20Electronics/PDF/L-24\(DK&SSG\)\(PE\)%20\(\(EE\)NPTEL\).pdf](http://www.nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Power%20Electronics/PDF/L-24(DK&SSG)(PE)%20((EE)NPTEL).pdf)