CARRIER OVERLAPPING PWM METHODS FOR ASYMMETRICAL MULTILEVEL INVERTER

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Abstract: Multilevel inverter has gained attention in recent years due to its high power capability associated with lower output harmonics. Several multilevel topologies have been reported in the literature and this paper focuses on asymmetric cascaded multilevel inverter employing Carrier Overlapping PWM (CO-PWM) technique. This technique provides reduced harmonics in the output voltage and significantly improves the root mean square value of the output voltage compared to the conventional Sinusoidal Pulse Width Modulation (SPWM). A detailed study of the proposed modulation technique is carried out through MATLAB/SIMULINK for Total Harmonic Distortion (THD). An experimental seven-level inverter test rig has been built to implement the proposed algorithm. Gating signals are generated using PIC microcontroller. The performance of the inverter has been analyzed and compared with the result obtained from theory and simulation.

Keywords: CO-PWM, Multilevel inverter, THD.

1. Introduction

MultiLevel Inverter (MLI) has been recognized as an attractive topology for high voltage DC-AC conversion. Several multilevel topologies are reported [Rodriguez et al (2000)] and the most popular topology is Cascaded Multilevel Inverter (CMLI) [Liao et al (2007)]. Normally, each phase of a cascaded multilevel inverter requires “n” DC sources for 2n+1 level. For many applications, multiple DC sources are required demanding long cables and this could lead to voltage unbalance among the DC sources [Zambra et al (2010)]. With an aim to reduce the number of DC sources required for the cascaded multilevel inverter for a motor drive, this paper focuses on asymmetric cascaded MLI that uses two unequal DC sources in each phase to generate a seven level equal step multilevel output [Manjrekar et al (2000)].

Several modulation strategies have been reported in the literature for the cascaded multilevel inverter [Calais et al (2001)]. This paper presents three types of carrier overlapping PWM methods that utilize the Control Freedom Degree (CFD) of vertical offsets among the carriers. They are COPWM-A, COPWM-B and COPWM-C. These three methods are simulated and compared for reduced harmonic characteristics in the output voltage. The effectiveness of the proposed modulation method has been carried out by MATLAB simulation. Both the MLI circuit topology and its modulation scheme are described in detail and their performance is verified based on simulation and experimental results.

2. Asymmetric Cascaded Multilevel Inverter

The proposed asymmetric cascaded multilevel inverter consists of two H-bridges. The first bridge H₁ consists of a separate DC source Vdc, whereas the second bridge H₂ consists of a DC source 0.5Vdc as shown in Fig.1. Let the output of H-Bridge-1 be denoted as v₁(t) and the output of H-Bridge-2 be denoted as v₂(t). Hence the total output voltage is given by v(t) = v₁(t) + v₂(t). By alternately opening and closing the switches S₁, S₄ and S₂, S₃ of H-Bridge-1 appropriately, output of H₂ v₁(t) can be made equal to +Vdc, 0 or -Vdc. Similarly the output voltage of H-Bridge-2 v₂(t) can be made equal to –0.5Vdc, 0 or +0.5Vdc by
opening and closing the switches of H2 [Zhong et al (2006)]. Hence \( v(t) \) takes values \(-1.5V_{dc}, -V_{dc}, -0.5V_{dc}, 0, +0.5V_{dc}, +V_{dc}, +1.5V_{dc}\) as shown in the Fig.2.

![Diagram of Asymmetric Cascaded Multilevel Inverter](image1)

**Fig.1 Asymmetric Cascaded Multilevel Inverter**

The advantages of the topology are reduced number of dc sources, high speed capability and high conversion efficiency [Mariethoz and Rufer (2002)].

![Voltage-time graph](image2)

**Figure 2 Seven-level output for asymmetric cascaded multilevel inverter**

The conduction table for the asymmetric cascaded multilevel inverter is shown in table 1.
Table 1 Conduction Sequence for Asymmetric Cascaded Multilevel Inverter

<table>
<thead>
<tr>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0.5V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
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<td>1</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1.5V_{dc}</td>
</tr>
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<td>0</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0.5V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-0.5V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-V_{dc}</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-1.5V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-0.5V_{dc}</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0V</td>
</tr>
</tbody>
</table>

3. Carrier overlapping PWM Modulation Technique

Several modulation techniques have been reported in the literature [McGrath and Holmes (2002)] for cascaded multilevel inverter. But this paper focuses on carrier overlapping PWM technique which provides reduced harmonic characteristics compared to the conventional PWM technique. Three Carrier Overlapping PWM (COPWM) methods that utilize the vertical offsets among carriers have been discussed in this paper. They are COPWM-A, COPWM-B and COPWM-C [Shanthi and Natarajan (2008)]. For an m-level inverter using carrier overlapping technique, (m-1) carriers with the same frequency(f_c) and same peak-to-peak amplitude (A_c) are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is 0.5A_c. The reference waveform has amplitude of A_m and frequency of f_m and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off [Azli and Choong (2006)].

3.1. COPWM-A Technique

The vertical offset of carriers for seven-level inverter with COPWM-A method is illustrated in Fig.3. It can be seen that the four carriers are overlapped with other and the reference sine wave is placed at the middle of the six carriers.
3.2. COPWM-B Technique

Carriers for seven-level inverter with COPWM-B method is shown in Fig.4. It can be seen that they are divided equally into two groups according to the positive/negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group.

3.3. COPWM-C Technique

Carriers for seven-level inverter with COPWM-C method are shown in Fig.5. In this pattern, the carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude-overlapped and neighboring-phase-interleaved carriers. Actually, pattern B and C have second control freedom change with the carriers horizontally phase shifted from pattern A besides the offsets in vertical.
4. Simulation Results

The above mentioned three types of carrier overlapping PWM methods have been implemented for asymmetric cascaded multilevel inverter and simulated in MATLAB/SIMULINK. The SIMULINK diagram of COPWM-A, COPWM-B and COPWM-C are shown in Figures 6, 7 and 8.
The simulated individual bridge outputs and the seven-level output waveform are shown in Figure 9.
From the simulation results, it is found that COPWM-A gives a reduced THD compared to the COPWM-B and COPWM-C and the THD values for various modulation index (m_a) for all the three PWM methods has been shown in Table 2. Therefore, COPWM-A has been chosen for asymmetric cascaded multilevel inverter.

Table 2 THD Calculation for various COPWM techniques

<table>
<thead>
<tr>
<th>Modulation Index (m_a)</th>
<th>%THD COPWM-A</th>
<th>%THD COPWM-B</th>
<th>%THD COPWM-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>9.02</td>
<td>22.6</td>
<td>12.13</td>
</tr>
<tr>
<td>0.9</td>
<td>9.10</td>
<td>26.0</td>
<td>13.45</td>
</tr>
<tr>
<td>0.8</td>
<td>9.69</td>
<td>29.99</td>
<td>15.75</td>
</tr>
<tr>
<td>0.7</td>
<td>10.65</td>
<td>35.90</td>
<td>19.78</td>
</tr>
</tbody>
</table>

The FFT spectrum for COPWM-A has been shown in Fig. 10 for m_a = 0.9
The root mean square value of the output voltage of COPWM-A for $m_a = 0.90$ is 17.83V, whereas it is about 11.01V for the conventional PWM (for $V_1 = 12V$ and $V_2 = 6V$) which clearly shows the advantage of COPWM-A compared to other PWM techniques. An LC filter ($L = 141$ mH and $C = 47$ uF) has been designed for the asymmetric seven-level inverter using the proposed COPWM-A technique and the filtered waveforms are shown in Fig. 11.

![Time (s) vs Voltage (V)](image)

**Figure 11**: Filtered output voltage waveform of asymmetric MLI

The FFT spectrum of the proposed COPWM-A with filter is shown in Fig. 12.

![FFT analysis](image)

**Figure 12**: FFT analysis for COPWM-A with filter ($m_a = 0.90$)

### 5. Experimental Results

This section presents the experimental results of the asymmetric seven-level inverter employing COPWM-A technique. PIC 18F4450 is used to generate trigger pulses for the semiconductor devices (IGBT) used in the circuit. The optocoupler used is 4N37, which is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photodetector. Fig. 13 shows the hardware set-up of MLI. Fig. 14 shows the experimental output waveform of seven-level inverter.
6. Conclusions

In this paper carrier overlapping PWM techniques have been analyzed for the asymmetric cascaded multilevel inverter. It is found that COPWM-A provides a lower THD and a higher DC bus utilization compared to other PWM techniques. A suitable LC filter has also been designed for the asymmetric topology which improved the harmonic characteristics of the load voltage. The combination of asymmetric MLI (which uses reduced number of DC sources) with COPWM-A can be used for electric vehicle applications. Also, DC source can be replaced by renewable energy source and the proposed topology can be employed for distributed generation.
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References