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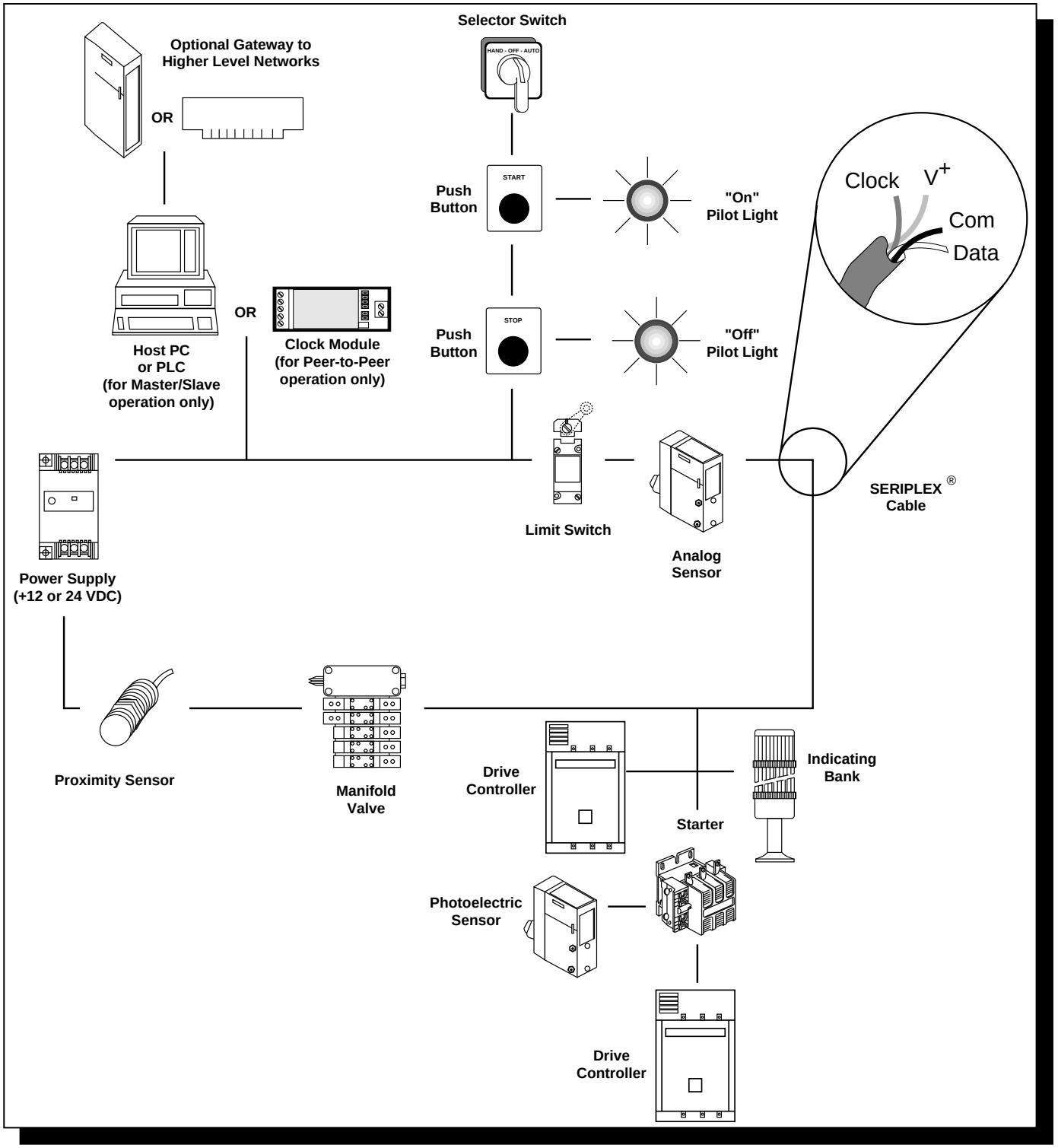
White Paper
Distributed, Intelligent I/O for Industrial Control and Data Acquisition … The SERIPLEX® Control Bus



PREFACE

With the advent of PLCs, a continuous stream of product enhancements and major new technologies have resulted in new processors, I/O devices, MMIs, etc., providing industry with major improvements in manufacturing control, plus a wealth of new process data that managers previously could only dream about.

However, there has been a price to pay – increasingly expensive control systems. Within the last few years, products such as small PLCs have brought the cost of processors down, but the cost of I/O still remains high. Efforts to develop new Fieldbus technologies, most of which use sophisticated communication protocols, may continue the upward price pressure on control system costs.

Many industrial managers are frustrated and impatient with the lack of progress toward usable solutions to reduce control system costs. However, the introduction of low level I/O networking systems that promote the distribution of I/O control close to the point of use holds considerable promise for future cost reduction.

INTRODUCTION

There are a few sensor and actuator networking approaches that offer simplicity and control system cost savings. These approaches, sometimes referred to as distributed I/O systems, are used to distribute sensors, actuators and pilot devices, such as proximity and photoelectric sensors, push buttons, pilot lights, contactors, solenoids, analog input and output devices in a cost effective manner throughout the control system, and often over very large distances.

Distributed I/O provides significant installation cost savings in wire, conduit, labor and start-up. With the reduction of local I/O and point-to-point parallel wiring, control panel enclosures are also significantly reduced in size and cost. Often, the costs of installation and start-up comprise as much as half the total cost of completed electrical control systems. Some very large companies are already using distributed I/O networks on an extensive basis because:

- Much less wire is required.
- The connection cost per device is a fraction of conventional installation cost.
- Installation and debug time is usually cut almost in half.
- Maintenance and fault determination are improved.
- Reliability and up-time are increased.

One of the most cost effective technologies in use today is the SERIPLEX® control bus. This technology is used by several manufacturers of sensors, actuators and terminating devices. Some of the companies developing and marketing products incorporating this technology are:

- Square D Company (SERIPLEX control bus)
- Turck (BusStop™)
- Pepperl+Fuchs (VariNet-3™)
- Banner Engineering (Photobus™)
- NAMCO (ProxBlox®)

The incentive for companies to use distributed control systems is strong. One survey estimates that over 67 million proximity sensors will have been put in use by 1995. It projects a growth to over 89 million annual usage by the year 2000. If you also include sensors for measurement of liquids, rigid materials, chemicals, thermal sensors, acoustic and other binary sensors, plus all the pilot devices and actuators that can be connected to a network, it is clear that huge potential savings can be achieved by distributing as much I/O as practical.

When selecting a distributed I/O system, there are a number of factors to consider:

1. Whether real devices in the form of I/O terminating modules or sensors and actuators are readily available in the marketplace.
2. Control system speed or response time required.
3. Length of the network and number of devices on it.
4. CPU platform that can be used, or whether the system stands alone and has its own logic capability.
5. Whether there is an installed base of qualified users.
6. Whether the system interfaces to other communication networks, LANs or WANs.
7. How the system installed cost compares to that of using conventional controls or competing networks.

"Installed cost" is really the cost benchmark to be considered. The base cost of the hardware devices is about the same as conventional hardware. The cost benefit received from using distributed I/O is really in the material and labor saved during installation and start up. Depending on the job, startup labor can be significant. Identifying and sorting out miswired connections when there are a couple of hundred pairs or more in a control system can be an extremely time consuming chore, to say nothing of the damage that can be done to the control system components from crossed wires and shorted circuits.

Distributed I/O systems are suitable for many types of applications. Some existing applications include:

- Machine tool control
- Material handling equipment controls
- Lighting control
- Assembly line monitoring
- Tank farm monitoring
- Automated inventory control
- Automated mining equipment remote controls
- NASA Mars Rover

Recently, several networking technologies for communicating with I/O devices have been introduced. However, most of these are actually high-level communication protocols residing above the level of the SERIPLEX control bus physical devices. As such, these systems have a more sophisticated protocol, are microprocessor-based and are more costly to implement. Additionally, they have slower response times, often unsuitable for real-time control. Most are not inherently deterministic, which is also an important requirement for industrial control systems.

Higher-level communication networks are, however, ideally suited for use in combination with the SERIPLEX control bus, interfacing via gateways or over the back plane of the CPU. They provide upper level, byte-type communication using packets of data not usually assigned to a component-level, bit-type network like the SERIPLEX control bus.

It is interesting to study the differences between bit and byte-level systems. By noting the key differences between their bus structure, bus scan times, determinism, data packet transfer size, etc., it can be seen that byte-type systems are excellent for higher level communication, and bit-type systems are ideal for simple, physical level I/O devices such as sensors and actuators. Table 1 on page 21 compares several byte and bit-level systems, including the SERIPLEX control bus.

The SERIPLEX control bus technology was developed by Automated Process Control, Inc. (APC), in Jackson, Mississippi. Robert Riley, Vice President of Engineering and Product Development, received the first patent awarded on the system in 1987. The SERIPLEX technology was specifically developed for industrial control applications. It accommodates several thousand I/O devices on a single network, extending over 5,000 feet. Both analog and digital (binary) devices can be controlled and monitored on the network. Small SERIPLEX chips are embedded in sensor and actuator devices, providing direct connection to the bus.

Over the last several years, this technology has demonstrated its ability to provide major control system cost savings. According to users, these savings reduced installation and startup costs by as much as 50% to 70% compared to conventional wiring methods.

SYSTEM DESCRIPTION

The SERIPLEX control bus is a deterministic, serial multiplexed, intelligent, distributed I/O system, providing both master/slave and peer-to-peer I/O control and logic.

The SERIPLEX network cable connects to I/O devices in one of two ways:

- Directly to devices that contain an embedded SERIPLEX ASIC (Application-Specific Integrated Circuit)
- Through general-purpose I/O blocks that contain the SERIPLEX ASIC

The ASIC, or “chip”, provides the communication capability, addressability and the intelligence to execute logic in virtually any sensor or actuator. The control bus supports both binary (discrete or digital) and analog device communication.

Hardware and installation cost savings are achieved by placing I/O blocks as close to the point of I/O device use as possible. Communication takes place over a four-wire, low-voltage cable. The SERIPLEX control bus eliminates the thousands of parallel wires usually run through conduit from local control cabinets to I/O devices, such as thermocouples, push buttons, proximity switches, photoelectric sensors, valves, solenoids, contactors, thermal sensors, etc.

In addition to the material cost savings, there are significant labor savings as well. The labor cost to install a small, four-wire cable the size of a little finger that does not require conduit, is a mere fraction of the cost of installing conduits, pulling a multitude of control wires through them and then trying to identify and terminate the individual circuits.

The SERIPLEX control bus transmits both digital and analog I/O signals in real time for both control and data acquisition applications. It combines distributed and local I/O capability on the same bus.

The control bus is designed to complement rather than compete with the higher-level, more sophisticated protocol, Fieldbus-type communication systems that are best suited to transmitting large information data packets. It resides primarily at the physical device level, providing the deterministic, process-critical, real-time I/O updates needed by most control systems, and leaves higher-level communication that does not require fast response time to others.

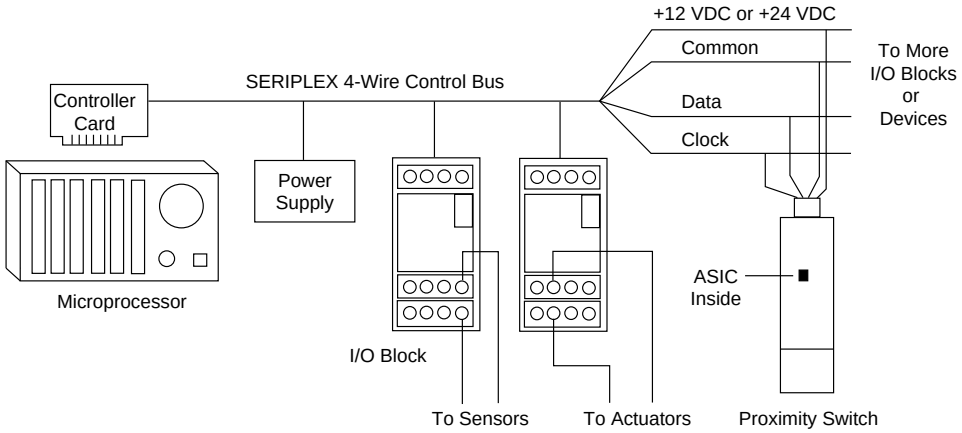


Figure 1 Typical Computer (Master/Slave) Configuration

A basic Master/Slave configuration includes a host CPU, an interface card to provide a communication signal source, a power supply and some I/O blocks and/or I/O devices with the SERIPLEX ASIC embedded in them (see Figure 1). Connecting these components is a four-wire cable with two conductors for communication and two for the network power.

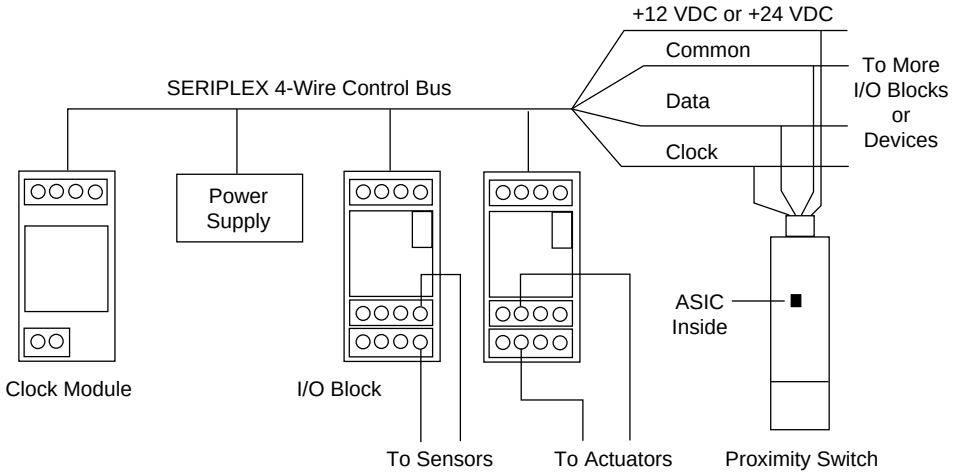


Figure 2 Typical Peer-to-Peer (Module-to-Module) Configuration

A Peer-to-Peer or stand-alone configuration (Figure 2) does not use a CPU at all. It simply requires a clock module for the communication synchronization source, a power supply, I/O devices, and the cable.

The power of the control bus lies in its capacity to control over 7,000 binary I/O points, or 480 analog signals (240 input plus 240 output), or some combination of discrete and analog I/O through one small four-wire bus cable. This eliminates the hundreds of point-to-point wire pairs often seen in a control system, run from a control cabinet through conduit.

The SERIPLEX control bus cable may be configured as a ring, a star, multi-drop, daisy-chain, loop-back, or in any topology combination desired (see Figure 3).

Operation differs substantially from other multiplexed systems because addressing, communication capability, and logic functions are programmed directly into on-board, non-volatile memory elements. The communication capability is inherent in the I/O block or device, rather than relying on a microprocessor for this function—there is no microprocessor in the SERIPLEX ASIC.

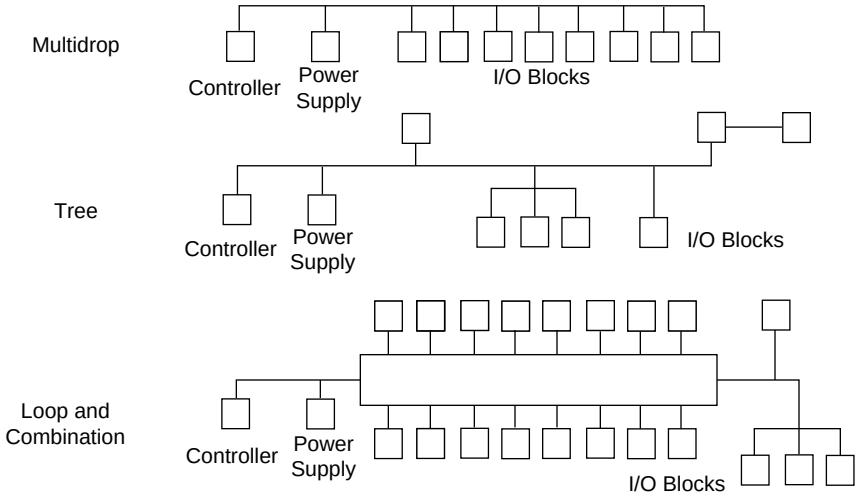


Figure 3 Sample SERIPLEX Control Bus Configurations

In the case of input devices, such as sensors, with an embedded SERIPLEX ASIC, the only connections needed are directly to the SERIPLEX bus (See prox switch in Figures 1, 2 and 4). There is no additional wiring necessary. Power for the sensor can usually be furnished by the two bus conductors supplying DC power. Actuators with the embedded ASIC also connect directly to the SERIPLEX bus. However, good engineering practice dictates that actuator devices be powered from a separate power source to avoid defeating the devices' optical isolation.

Two of the four conductors in the shielded, four-wire bus cable deliver +12 VDC power or +24 VDC power (user's choice) to the bus. Bus voltage for systems using devices or modules with first-generation ASICs are restricted to +12 VDC power only. The other two conductors provide communication to and from the modules and devices. One of the communication lines is for a data signal and the other for a clock signal that controls network timing. The shield usually has a drain wire.

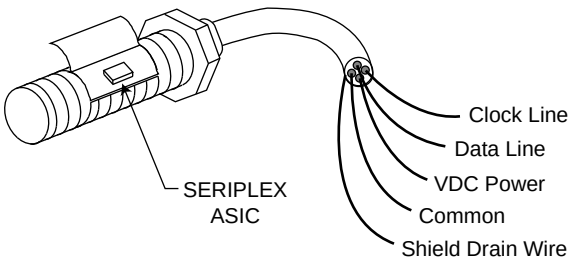


Figure 4 Proximity Switch with ASIC Built-In

HOW THE BUS WORKS

The heart of the control bus is the SERIPLEX ASIC. This application-specific integrated circuit is embedded in I/O devices or I/O blocks. It supports communication between I/O devices and the host CPU over the SERIPLEX control bus.

In the Master/Slave mode (sometimes referred to as Mode 2), the ASIC provides for the communication of organized field events, occurring at the I/O devices, to a host CPU, to be acted upon by the application program resident in the host.

In the Peer-to-Peer mode (sometimes referred to as Mode 1), there is no host CPU. The events occurring at each device are communicated directly between I/O blocks or devices containing an embedded ASIC. These events are acted upon at the device level and are based on the logic functions programmed into the ASICs.

The data signal is simple and basic in nature. It utilizes large signal swings (12 V peak to peak), low-pass filtering, and large hysteresis to maintain data integrity. There also is a provision for redundancy at the inputs to provide even further data protection, plus a bus fault detection scheme for additional data integrity.

The cable used for the SERIPLEX control bus is a special design, but available from several manufacturers. The basic design consists of two AWG #22 communication wires, for clock and data signals. There are two additional AWG #16 wires for the power and common conductors.

The wires have an overall shield with a drain wire and are covered with an overall jacket. The cable is designed for low capacitance to achieve maximum communication distance and speed.

The capacitance in the cable has a direct effect on the distance of communication and the speed of communication. Using one of the standard cables rated at 16 pF per foot, maximum communication distance at 100 kHz clock rate is approximately 500 feet. Maximum communication distance with the same cable at 16 kHz is about 4800 feet. A cable with 20 pF per foot limits communication to about 350 feet at 100 kHz, and 3900 feet at 16 kHz.

There are variations of the basic cable, such as special application ratings or additional pairs of conductors to provide separate power to actuators. Cable data sheets are available. The cables are available from multiple manufacturers.

ASIC General Description

There are two versions of SERIPLEX ASICs. The two are similar in function and the second-generation SPXSP256-2B is downward compatible with the first generation SPX-256 ASIC. They can both reside on the same system, as long as the bus voltage is +12 VDC. The SPXSP256-2B also operates at +24 VDC.

The ASICs are programmed differently. The first generation ASIC requires a programming port on the I/O block or I/O device into which it is embedded. The SPX-SP256-2B is programmed by connecting the programmer to the four bus conductors. This is an economical connection that does not require additional real estate for the programming port.

ASICs are generally programmed with a hand held Set-Up Tool for addresses, logic function and mode of operation. Addresses are entered as integer numbers at the Set-Up Tool's address prompt. Each ASIC has two physical inputs (A & B) and three physical outputs (A, B & C). Logic is programmed by setting each input and output point in the ASIC to a normally-inverted or non-inverted state by means ofthe ASIC's on-board non-volatile memory.

The C output is available as a logical function of the A and B outputs. Unlike the A and B outputs, Output C is not directly addressable from the bus. Generally, either the C or B output may be used on an I/O block. This selection is usually made via a jumper located on the I/O block. The choice of B or C output on an I/O device with an embedded ASIC is usually set at the design level within the device.

Additional logic functions can be programmed into the second-generation ASIC. One of these enhancements, Digital Debounce, allows for sampling data once, twice, or three times on consecutive bus scans. The data must be identical on each of the selected number of scans before it is passed on to physical outputs.

Both ASICs can operate in Master/Slave or Peer-to-Peer mode. This is determined at the time of programming. This selection determines how the ASIC handles data. Figures 5 and 6 show a simplified block diagram of its functions in the two modes.

In the Master/Slave mode, data is passed from the inputs to the data line and delivered to the host CPU application program, so that it is acted upon based on the logic in that program. The result of that logic is transmitted over the data line to turn output devices on or off as appropriate.

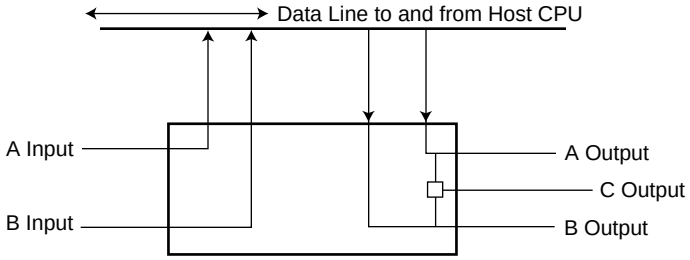


Figure 5 Master/Slave ASIC Block Diagram

In Master/Slave mode, the status of the inputs at various addresses determine the action of outputs at various addresses, based on the logic in the application program residing in the host CPU. Although inputs and outputs have complementary addresses (that is, they receive the same numerical address number) there is no direct logical relationship between the inputs and outputs on the same ASIC. This is controlled strictly by the application program logic.

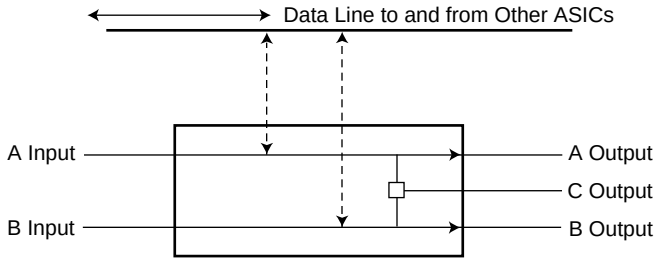


Figure 6 Peer to Peer (ASIC to ASIC) Block Diagram

The ASIC behaves quite differently in the Peer-to-Peer mode. In Mode 1, inputs at a particular address have a direct effect on outputs with the same numerical address. In Figure 6, the solid lines going from the input to the output represent this direct logical effect between inputs and outputs at the same address.

The status of the A and B inputs, and the A, B, and C outputs can be programmed to be either inverted or non-inverted in their normal (inactive) state. Each is programmed individually. This provides 32 Boolean logic combinations.

Inputs and outputs with the same address do not have to be in the same location, and in fact, seldom are. The output can be in a device several hundred feet away from the input. As long as they have the same address, any action at an input has a direct effect on all outputs on the bus with the same address as the input.

The broken lines with arrows, shown in Figure 6, represent the status of the inputs and outputs at each address reflected to the data line. This is useful when running in Peer-to-Peer mode using a CPU interface card. SERIPLEX CPU interface cards can be configured for either Mode 1 or Mode 2 operation. The host CPU can follow the status of each of the I/O points, in peer-to-peer mode, even though the logic is being executed at the I/O level.

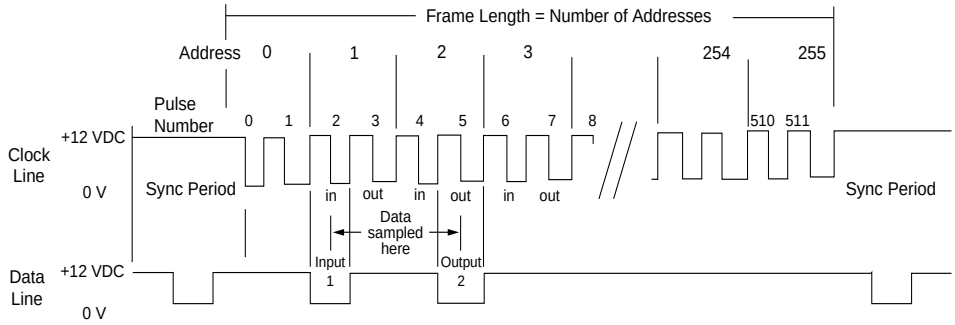


Figure 7 Master/Slave Timing Diagram

Master/Slave Mode

- A synchronizing signal is generated on the clock line by one of the various types of interface cards available. It is typically 8 clock cycles long and synchronizes all devices in the system (see Figure 7). On the first negative-going (logic high-to-low) edge of clock pulse number 0, the system becomes active. All ASICs on the control bus are synchronized and waiting for the first positive clock transition to open the data window.
- The sync pulse is followed by up to 512 clock pulses. Each pulse corresponds to an input or output address on the bus. There are 256 numerical addresses on the bus. Address 0 is reserved for use by the system, while addresses 1 through 255 are availble for the user. During the sync period, certain bus "housekeeping" activities take place, such as checking to see that the data line is operational. If not operational, outputs revert to their inactive states.
- Complementary addressing provides an input and output at each numerical address. The pulses are counted by the ASIC embedded in each I/O block or device connected to the bus.
- In Master/Slave Mode, when the number of pulses received by an I/O block or device equals two times the address it was programmed for, that module or device is given access to the data line. The status of input is communicated to the host CPU via the data line and the condition of the output is set according to the application program in the host CPU.
- When all the address clock pulses have been sent, up to a total of 512 , the synchronizing signal is generated again and the operation repeats itself.
- Clock frequencies from 16 kHz to 100 kHz are selectable on Version 1 host interface cards and clock modules. Clock rates from 10 kHz to 200 kHz are supported by Version 2 I/O devices and interface cards.

- If all 256 available addresses are scanned on a Master / Slave system, and a clock rate of 100 kHz is selected, the scan time of the bus is 5.2 ms and the response time to scan all inputs and set all outputs is about 16.2 ms. If faster response times are required, a selection can be made on the interface card or clock module to scan less than the full 256 addresses. This selection is made at 16-address intervals (16, 32, 48, etc.).
- Frame length is the number of addresses scanned on the control bus, and can be any number between 16 and 256, in multiples of 16.
- Bus Response Time for a Master / Slave Configuration can be estimated from the following formulas:

Bus Input Response Time – input to processor (in seconds):

$$\frac{(2 \times \text{Frame Size}) + 40}{\text{Clock Frequency}}$$

Bus Output Response Time – processor to output (in seconds):

$$\frac{(4 \times \text{Frame Size}) - (2 \times \text{Output Address}) + 48}{\text{Clock Frequency}}$$

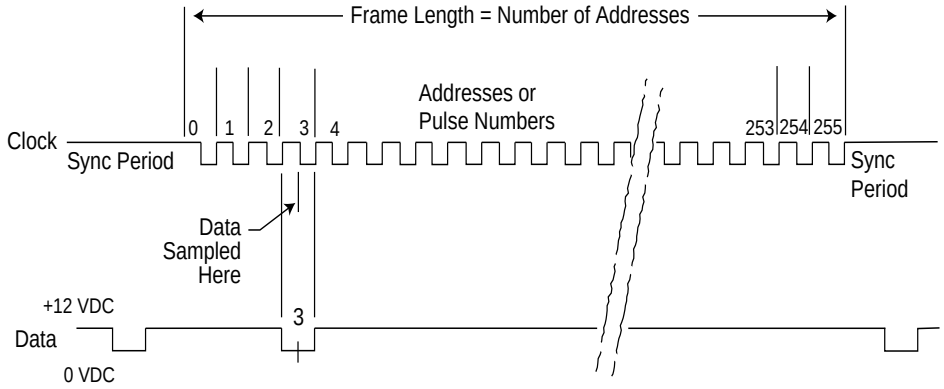


Figure 8 Peer-to-Peer Timing Diagram

Peer-to-Peer Mode

- A synchronizing signal is generated on the clock line by a interface card or clock module. It is typically eight clock cycles long and synchronizes all devices on the control bus. See Figure 8.
- The sync pulse is followed by up to 256 clock pulses. Each pulse corresponds to an address on the bus. Although there are 256 addresses on the bus, only 255 are available to the user. Address 0 is reserved, leaving addresses 1 through 255 for the user. Complimentary addressing provides an input and output at each address. The pulses are counted by each module or device connected to the bus.
- When the number of pulses received by an I / O block or device equals the address it was programmed for, that I / O block or device is given access to the data line. The status of inputs is communicated to outputs with the same, but complementary, address via the data line. The condition of the output is set according to the Boolean logic programmed into the I / O block or device. In this mode, inputs have a direct effect on outputs with the same numerical address.
- When all the address clock pulses have been sent (up to a total of 256) the synchronizing signal is generated again and the operation repeats itself.
- Frame length is the number of addresses on the control bus, and can be any number between 16 and 256, in multiples of 16.

- Bus Response Time from an input event to an output changing state for a Peer-to-Peer System can be estimated from the following formula:

$$\text{Time in seconds} = \frac{(2 \times (\text{Frame Size} + 8)) - \text{Address} + 0.5}{\text{Clock Frequency}}$$

BUS AND DEVICE FAULT DETECTION

Because many devices can be connected to the same bus cable, a fault within the cable or any device can have a widespread effect on the system. Therefore it is essential for a component-level network to provide effective diagnostic capability, so that any problems can be identified and corrected quickly and easily. For this purpose, the SERIPLEX bus provides several methods to help detect and isolate problems with bus cable and devices. These methods include:

- Host interface cards continually monitor the bus cable and report fault conditions such as shorts among the 4 bus conductors, or excess capacitance in the bus cable.
- Each I/O device on the bus tests the bus integrity at the end of every data frame by monitoring a "Bus Fault Detection" pulse transmitted by the interface card. Failure to properly detect this pulse implies a problem with the bus power or with clock or data signals, and the devices reject the last frame's output data and immediately set their outputs to their default "shelf states".

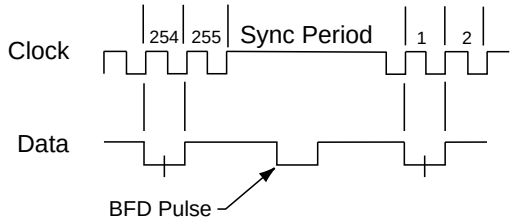


Figure 9 Bus Fault Detection (BFD) Pulse

- Any I/O device can be used to detect bus open-circuit conditions by setting it up to continually report a signal at any unused input address. These devices can be placed at different points along the bus cable to isolate the location of any open-circuit problem. Through use of the Data Echo feature, more sophisticated detection of all types of bus faults (shorts, opens, and excess capacitance) can be performed.
- Ordinary I/O devices can be configured to report their presence and health simply by making use of a spare input signal. In addition, device vendors can incorporate special device diagnostics to indicate conditions such as marginal detection from a photo eye, or welded contacts on a relay.

DATA ERROR AVOIDANCE AND DETECTION

Since it connects directly to sensors and actuators, the SERIPLEX bus cable may be subjected to electrical noise from a variety of sources. It is important to prevent this noise from affecting the operation of a control system.

Obviously, the best way to respond to electrical noise impulses is to ignore them completely -- that is, to prevent them from causing an invalid data transmission. The SERIPLEX bus employs a variety of methods which allow it to avoid disruption more effectively than almost any other control network available. These methods include:

- An unusually wide 12V signal amplitude, coupled with 4.5V hysteresis, to effectively "drown out" most noise impulses
- A shielded cable, with bus power isolated from other electrical circuits, to greatly reduce the amount of noise coupled onto the bus cable

- Relatively low operating frequency due to highly-efficient protocol, which allows filtering of noise at frequencies where other control networks must operate to achieve acceptable response time

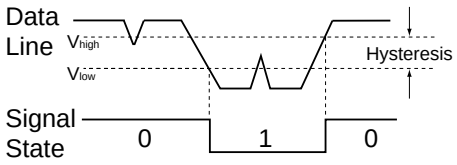


Figure 10 Hysteresis

Of course, no bus is completely immune to disruptions. For this reason, the SERIPLEX bus provides several methods to detect whether data transmission errors have occurred, so that a correction or other appropriate response can occur.

The error detection methods of typical control networks are not appropriate for the simple SERIPLEX bus. Since most signal transmissions are only one bit in length, adding parity or a CRC (Cyclic Redundancy Check) to each signal is too costly both in time and complexity. A CRC encompassing the whole data frame might provide reasonable error checking, but would need to halt data transmission among all devices if any one device experienced an error. Therefore the Seriplex bus provides simple and efficient error detection methods which can be applied to individual data signals:

- The Digital Debounce feature provides a receiving device with verification that it has received a single-bit signal correctly. When this feature is enabled, the device must see 2 or 3 identical data samples before changing its signal state, effectively filtering out both spurious noise and electromechanical contact bounce.
- The Data Echo feature provides a sending device with verification that a single-bit signal has been received correctly by another device. The receiving device "echoes" an output signal by retransmitting it to the bus as an input signal.
- CDR (Complementary Data Retransmission) provides a receiving device with verification that it has received an 8- or 16-bit signal correctly. The data is retransmitted through a special encoding process, which also verifies that it is being transmitted at the right address and multiplex channel. Upon detection of an error, the receiving device can take appropriate action such as rejecting the data or notifying other devices.

In keeping with the SERIPLEX philosophy of simplicity, all data error detection methods are optional. This means that they can be selectively applied to only the signals which require them—non-critical devices and systems need not be burdened with unnecessary overhead and complexity. Further, these methods can frequently be implemented without affecting the response time of the SERIPLEX bus. When enabled, these methods provide an efficient and effective means of data verification for critical signals and processes.

THE CPU INTERFACE CARDS

The host CPU (PC XT / AT, VME, STD, Multibus I and II, PC / 104, EXM or any custom system) is linked to the bus by a host interface card (Figure 11). Each interface card can support over 7,000 digital input and output addresses or 240 analog input plus 240 output analog signals, or some combination of digital and analog devices. Multiple interface cards can communicate with a single host CPU for expanded I / O requirements.

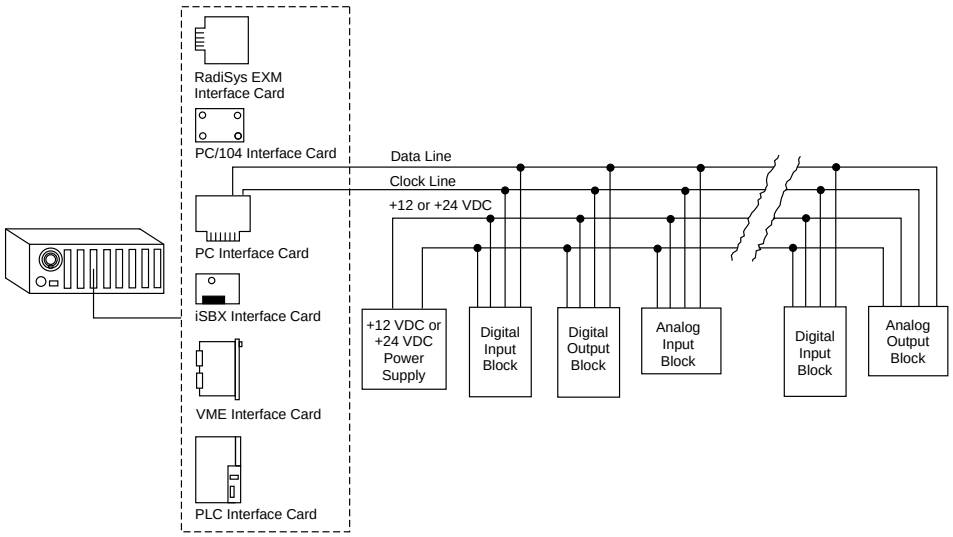


Figure 11 Host Interface Card and I/O

Interfacing to a custom CPU is not difficult because of the simple design used. It is readily adaptable to almost any microprocessor, even board-level types. Regardless which host is used, a design concept common to all interfaces makes it simple … the use of dual-port RAM.

Figure 12 shows a block diagram for current-design interface cards. The host CPU looks at bits in dual-port RAM to see the status of inputs, or writes to them to turn outputs on or off. Each bit represents one digital I/O point.

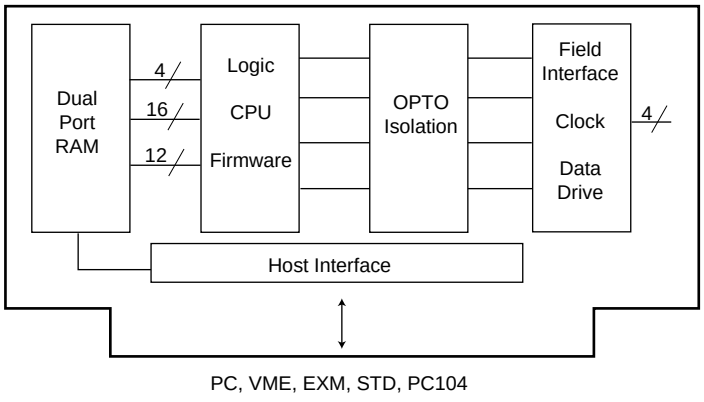


Figure 12 Block Diagram of Host Interface Card

The interface card is a co-processor card. It has an on-board processor that manages the SERIPLEX network, keeping track of the addresses in use, logic functions, status and the protocol "housekeeping" functions. This means that the application software designer does not need to understand the SERIPLEX protocol—one need only be concerned with the status of bits in memory. A programming library for C language is provided for developing the link between the host processor and bus and the interface card for those developing custom programs.

There are a number of third-party software suppliers that provide application program software packages with built-in drivers for the SERIPLEX interface cards. These software products include:

- FloPro®
- 86Ladders™
- Wonderware®
- Gello®
- Steeple Chase™
- Omega Controlware™
- PowerMac System 1000™
- Genesis™
- SoftPLC®.

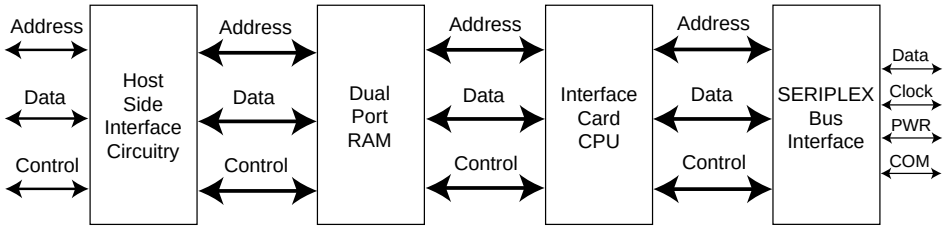


Figure 13 SERIPLEX Interface Card Block Diagram

Figure 13 shows how SERIPLEX interface cards interface to the host CPU on one side and to the SERIPLEX control bus on the other. There are four main areas on each SERIPLEX interface card: the host CPU interface circuitry, the dual-port RAM, the on-board CPU, and the interface circuitry to the SERIPLEX control bus.

The dual-port RAM on the interface card appears to the CPU as a 2k block of memory. The engineer assigns the location of that memory to the host CPU when the card is initially installed, and it is accessed just like any other memory. The memory is partitioned for various uses to provide extensive administrative control.

Dual-port RAM is divided into three segments:

- Data
- Status
- Control

The **data segment** contains the NON-MUX (non-multiplexed) INPUTS and OUTPUTS data areas, the SAFE STATE buffer, and the MUX INPUT and OUTPUT BUFFER areas. See Figure 14.

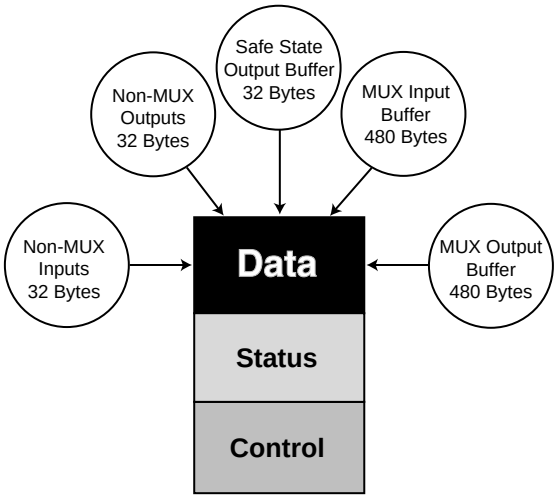


Figure 14 Dual-Port RAM – Data Segment

A unique feature of the dual-port RAM system is that both binary and analog signals can be multiplexed on the bus. This feature is usually used to provide up to 240 analog inputs plus 240 analog outputs on the same bus, or some combination of analog and binary I/O. This data is stored in the dual-port RAM on the host interface card.

It is possible to extend the multiplexing capability of the control bus to accommodate 7,680 binary I/O points. Consistent with the complementary addressing scheme, this provides 3,840 inputs and 3,840 outputs. Analog values can easily be mixed with binary I/O. They each consume 8, 12 or 16 binary bits, depending on the resolution desired.

Each of the dual-port RAM areas are defined in terms of a bit table. Each bit in an area represents a SERIPLEX address and is stored within a byte quantity of memory. Multibit values, such as an analog or counter value, can also reside in this area. They are registered as a continuous group of address bits.

The **status segment** of the dual-port RAM has two basic areas (Figure 15). The CONFIGURATION ID status area contains product and firmware revision status information. INTERRUPT, OPERATIONAL and ERROR STATUS areas contain information regarding the status of interrupts, operation modes and parameters, and error indications.

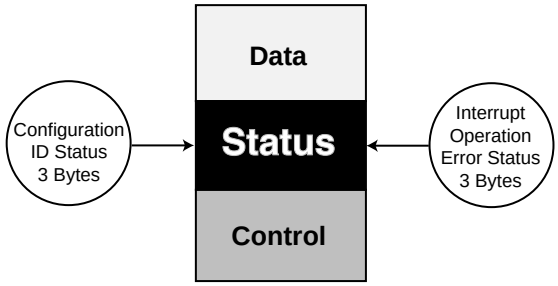


Figure 15 Dual-Port RAM – Status Segment

The STATUS BYTES contain information about the error status of the SERIPLEX control bus (current or bus faults), product ID codes and firmware revision codes.

The **control segment** of the dual-port RAM also has several areas for specific functions (Figure 16).

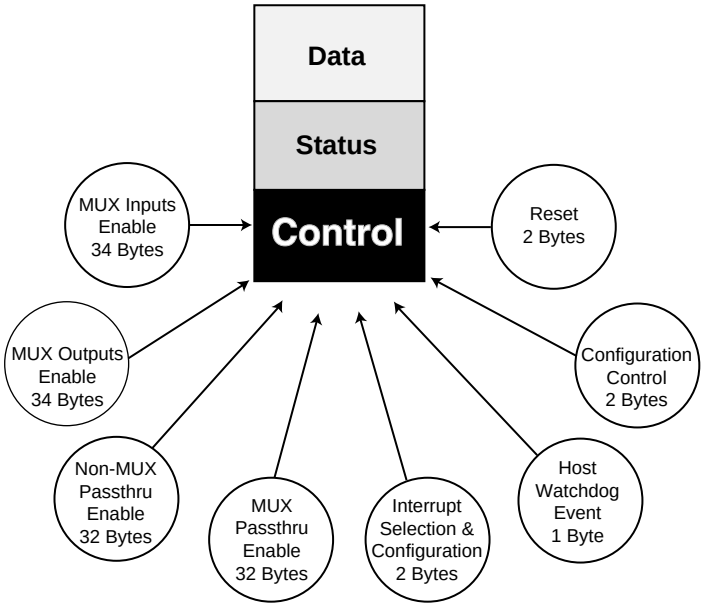


Figure 16 Dual-Port RAM – Control Segment

The MUX INPUTS ENABLE is used to indicate which of the input blocks of SERIPLEX bus addresses are to be used in the multiplex mode of operation. This allows the application designer to define up to 15 multiplex blocks on a single bus (see Figure 17).

The MUX OUTPUTS ENABLE is used to indicate which of the OUTPUT blocks of SERIPLEX addresses are to be used in the multiplex mode of operation. Output data can be multiplexed independently of whether input data at the same address is multiplexed.

The NON_MUX PASS_THRU is used to indicate which of the non-multiplexed SERIPLEX address INPUTS are "passed through" directly to the SERIPLEX address OUTPUTS. This is a feature in Master / Slave mode that allows the action at an input device to cause an action at an output device having the same address, without the data going through the logic in the application program in the host CPU. This provides a faster response time (at Mode 1 speed) for update of output devices.

Similarly, the MUX PASS_THRU is used to indicate which of the multiplexed SERIPLEX address INPUTS will be "passed through" directly to the SERIPLEX address OUTPUTS.

The INTERRUPT SELECTION AND CONFIGURATION area is used to select which level of interrupt request is used for interrupting the HOST CPU, and to identify what event will cause the interrupt.

The HOST WATCHDOG EVENT is used to indicate that there is not a communication fault between the host CPU and the SERIPLEX interface card. A byte is written to this area of dual-port RAM from the host CPU each scan to indicate that the host is communicating.

The CONFIGURATION CONTROL area is used for setting up parameters such as bus clock rate, multiplex channel size, multiplex priority channel, etc.

The RESET area is for using the hard reset feature to reset the SERIPLEX interface card.

The operating manual, furnished with each interface card, provides complete instructions on set up and use, including sample C code where applicable.

Figure 17 illustrates how multiplexed addressing is set up and appears on the bus. Address 0, which follows the sync signal used to reset all address counters in the ASICs in each scan is not used to transmit data. The binary value of the following bits (1, 2, 3 and 4) determine the multiplex channel which will be scanned in that particular data frame. I/O devices which are assigned to that particular multiplex channel will communicate with the bus during that frame, while devices which are assigned to other multiplex channels will not. Non-multiplexed devices communicate every frame, regardless of the multiplex channel being scanned.

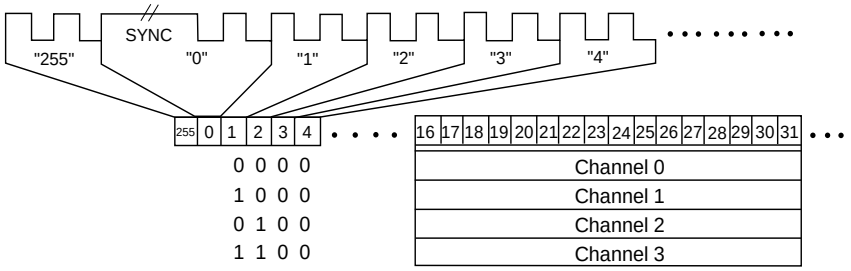


Figure 17 Four-Channel Multiplexed Addressing

Figure 17 shows the selection of the “multiplexed address block”at addresses 16 through 31. The next address block available is 32 through 47, and so on at each 16-bit address boundary (see Figure 18). The “channel” is selected via the binary value at output address bits 1, 2, 3 and 4. The SERIPLEX control bus allows the number of multiplex channels to be set at 2, 4, 8 or 16 for each interface card. The number of channels shown in Figure 17 is 4, channels 0 through 3. Figure 18 shows 16 channels, channel 0 through 15. This design feature allows for up to 15 blocks of 16 channels on each SERIPLEX network.

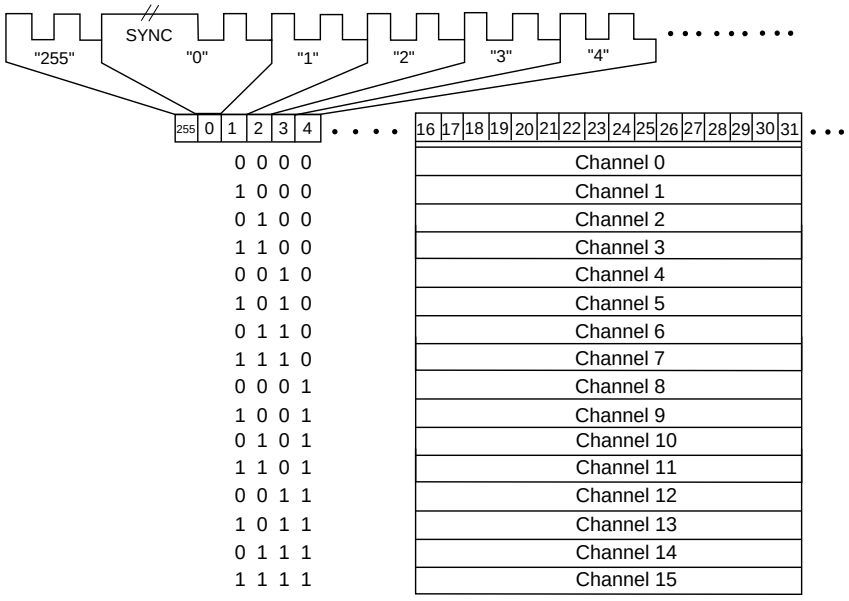


Figure 18 Sixteen-Channel Multiplexed Addressing

Standard analog I/O blocks currently offered take full advantage of the available multiplex addressing capability on the SERIPLEX control bus. A total of 480 analog signals (240 input plus 240 output) are available using the multiplex addressing.

If all available multiplexed addresses are used, a total of 7,680 binary I/O signals, or some mix of binary and analog signals is available. The maximum number of usable discrete I/O signals per network is 510 without multiplexing. The control bus is limited by how much power it can support, which is directly related to the size of the cable conductors, the bus length and power supply used.

It is also possible to select any one of the multiplex channels as a priority channel. This selection forces the system to scan that channel and make its updated data available to the host CPU every second frame.

If a priority channel is not selected, each channel is scanned successively in ascending order. If four channels are set up for multiplexing, it takes four frames to read the data in all four of the channels. Signals which are not multiplexed are still updated every frame.

It should be noted that reference has always been made to the number of addresses available and not the number of I/O that can reside on the network. Multiple I/O blocks and devices can be used at all addresses if the I/O action is required in multiple locations, every time a device at that address is given a command. For instance, if multiple lights are used in various location to indicate the same condition, they can all be assigned to the same address, and activated with a single signal.

If more I/O is required than one host interface card can provide, a solution is to add additional host interface cards. Any number of additional cards may be added; the only restrictions are the memory of the host CPU, and the number of backplane slots available.

I/O DEVICES

There are few limitations as to what kind of I/O blocks can be designed. Although there are standard catalog devices available, some OEMs design devices specific to their own applications. The ASIC is very simple to adapt to custom I/O blocks, which can resemble terminal blocks, or directly into sensors and actuators.

Several companies manufacture devices or have products in the planning stage incorporating the SERIPLEX ASIC, such as Banner Engineering (photo sensors), Pepperl+Fuchs (proximity switches), NAMCO, Square D Company, Turck, etc. Applications include embedding the ASIC in valve manifolds and bodies, contactors, grippers, process instrumentation, and other actuators, sensors and pilot devices.

For applications requiring local I/O, high-density analog and digital I/O boards are available. These provide a large number of I/O at a single location. Up to 48 digital and 32 analog I/O are available in a small package with only one SERIPLEX bus connection required for each group of I/O. Custom mixed signal I/O cards combining large quantities of discrete and analog I/O on a single card have also been designed into process machinery. They connect to the same control bus as the more highly distributed block-style devices and can be mixed with the block-style devices.

Standard-style I/O blocks are available from multiple sources in a variety of configurations. They are small, compact and facilitate installation close to the I/O devices to which they are connected.

Both AC and DC blocks are available with as few as two input channels or two output channels per block, or as high as 8 input channels per block or 8 outputs per block. There are also combination blocks with two inputs and two outputs per unit. Generally, these are used as smart terminal blocks for connecting "dumb" standard devices to the SERIPLEX control bus.

Eight-bit and twelve-bit analog input and analog output blocks are available in a variety of designs. Conditioning modules, which plug into them, handle various types of signals.

Analog-to-digital (ADC) and digital-to-analog (DAC) conversions, made at the block, enhance the integrity of the transmitted signal (see Figure 19). Analog input blocks convert the analog signal to a digital value for transmission over the SERIPLEX control bus. Resolutions available are 8, 12 and 16 bits.

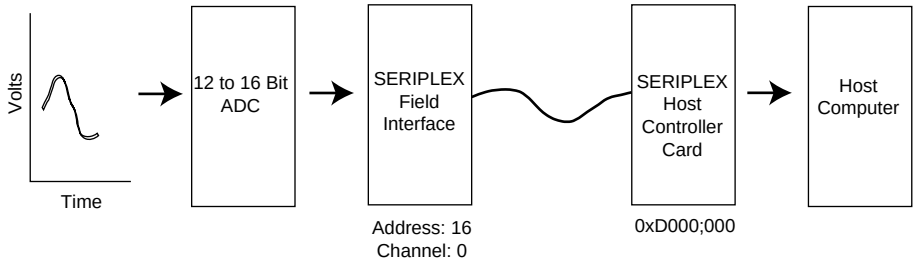


Figure 19 Analog to Digital Conversions

If used in the Master / Slave mode, the digital value is received at the host CPU by the SERIPLEX interface card, where the value is written to its defined address location in the dual-port RAM. The value is then usable by the application program in the host CPU by accessing the appropriate bits in dual-port memory.

Analog output blocks reverse the process, receiving a digital value stored in the dual-port RAM of the SERIPLEX interface card from the SERIPLEX bus. This value is read by the SERIPLEX I / O block with the associated address, converted within the block to a corresponding analog value and transmitted to the field device controlled by this signal.

OPEN ARCHITECTURE

The SERIPLEX control bus is offered as an OPEN TECHNOLOGY through a simple one-page licensing program. It is very easy and inexpensive to embed the SERIPLEX ASIC, and does not require the purchase of an expensive development system.

A development system which includes 10 ASICs, a Set-Up Tool, and an I / O circuit design manual, is available upon signing the simple participation agreement. The information necessary to design an interface card or an ASIC programmer is also available.

The licensing program is open to those who desire to develop products that can communicate over the SERIPLEX control bus. Technical information and support is available to those wanting to develop interfaces to custom CPUs.

The SERIPLEX ASIC is available to companies wishing to embed the ASIC into their sensor or actuator devices from Square D or directly from the IC foundry, American Microsystems Inc.

For more information regarding the use of SERIPLEX technology or to incorporate the ASIC in your products, contact the SERIPLEX Technology Organization, Inc. (STO) at 1-800-SPLXINC (1-800-775-9462).

As a result of the open technology philosophy, the SERIPLEX ASIC can be combined with other communication networks at the IC level, either as silicon or using a multi-chip configuration, or by use of a communication gateway device. The interfaces to various field buses are simplified through the use of dual-port RAM by the SERIPLEX CPU interface card.

The SERIPLEX control bus system is the least-expensive, easiest, and simplest-to-implement network for providing communication to both distributed and local analog and digital I/O available today. By far, it offers greater installation cost reduction for distributed I/O than any other system currently available, along with the largest industrial installed base of any control bus on the market.

FEATURE COMPARISONS

Table 1 Feature Comparison of I/O Networks – ASI, SERIPLEX, SDS™ CAN bus, DeviceNet™ CAN bus

Feature	ASI	SERIPLEX	SDS CAN bus	DeviceNet CAN bus	TURCK SENSORPLEX®	LonWorks
Basic design	One chip for each sensor or actuator	One chip for each sensor or actuator	Several chips depending on application plus CPU support	Several chips depending on application plus CPU support	Master/slave stations	One programmable chip + transceiver for each network device
Operating voltage	24 VDC	12 VDC – 1st generation 12 or 24 VDC – 2nd generation	11-24 VDC	24 VDC supply 11-25 VDC at node	24 VDC	Varies, depending on transceiver type
Logic capability on chip	Cyclic on-off control	32 Boolean logic functions	CPU based – programmable	CPU based – programmable	Unknown	8-bit processor, C-language programming, up to 2K ROM
Device level error checking	Yes	Yes –CDR,digital debounce, & diagnostic output	Yes – 15 bit CRC, cyclic redundancy check	Yes – 15 bit CRC, cyclic redundancy check	FSK encoding/ filtering, no error detection	Yes – CRC
Method of operation	Master/slave	Master/slave and peer-to-peer	Master/slave Peer-to-peer proposed	Multi-master Peer-to-peer proposed	Master/slave	Peer to Peer
Number of devices per network	31 slaves (nodes) 124 binary devices	Non-multiplexed: 510+ (255 input + 255 output) Multiplexed: 7,680 discrete or 480 analog or a combination	64 nodes 128 binary/analog proposed	64 nodes 2,048 devices	32 stations, 192 total	32768
Bus scan time	5 ms for 31 slaves	Scalable – 0.72 ms for 31 sensors plus 31 actuators; 5.2 ms for 510 I/O devices	26 ms minimum for 32 devices	7.2 ms for 63 devices @ 500 kbaud 28.6 ms for 63 devices @ 125 kbaud	<5 ms for 192 I/O	30ms typical packet response
Inherently Deterministic	Yes	Yes	No – arbitration system	No – arbitration system	Yes	No
Addressing method	External DIP switches	Programmable EE element on chip	Software dependent on network	Software dependent on network	Physical on device	Software
Network structure	Trunkline-dropline only	Open – any combination of tree, loop, multi-drop, star, etc.	Trunkline – dropline only	Trunkline – dropline only	Master with daisy chain	Open – any combination of tree, loop, multi-drop, etc.
Network length without repeaters	Maximum 100 meters including drops	5,000 ft or longer	See Table 1a	See Table 1b	2,500 meters with amplifiers	5,000 ft. or longer, depending on transceiver type
Medium of transfer	Unshielded 2-wire power and signal	4-wire cable	4-wire cable	4-wire cable	Coax and IP67 connectors	Varies, depending on transceiver type – shielded cable, fiber-optic, etc.
Signal capability	Digital (binary) only	Binary, Analog, ASCII	Binary, Analog, ASCII	Binary, Analog, ASCII	Binary	Binary, analog, ASCII
Known interface cards	Siemens PLC	PC/AT, GE Fanuc 90-30 PLC, VME, EXM, PC/104, STDbus, A-B/GE/Modicon/Siemens via VME, SY/MAX PLC, Aromat PLC, serial	GE Fanuc 90-30	Allen-Bradley PLC	Siemens PLC, A-B PLC, others unknown	PC, VME, and many others
Market introduction	Fall 1993	1990	early 1994	mid 1994	USA 1992	1986
Working product	Fall 1994	1990	mid 1994	early 1995	USA 1992	1991
Additional Configuration on Bits	No	Yes	Yes	Yes	No	Yes
Data Packet Size	4 bits	1 – 255 bits	8 – 64 bits	8 – 64 bits	6 bits	1 – 250 bits

Table 1a SDS CAN bus

Data Rate (bits/second)	Max. Total Cable Trunk Length (ft)	Max. No. of Devices	Max. Branch Length (ft)
1,000 kbaud (1 Mb)	100	32	3
500 kbaud	400	64	6
250 kbaud	800	64	12
125 kbaud	1,600	64	24

Table 1b DeviceNet CAN bus

Data Rate	Distance	Drop Length	
		Max. Drop	Cumulative
125 kbaud	1,640 ft (500 m)	20 ft (6 m)	512 ft (156 m)
250 kbaud	820 ft (250 m)	20 ft (6 m)	256 ft (78 m)
500 kbaud	328 ft (100 m)	20 ft (6 m)	128 ft (39 m)

For more information regarding the use of SERIPLEX technology or to incorporate the ASIC in your products, contact the SERIPLEX Technology Organization, Inc. (STO) at 1-800-SPLXINC (1-800-775-9462).