

Study of ICP-CVD grown Amorphous and Microcrystalline Silicon thin films in HIT structure

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Abstract—We have investigated undoped hydrogenated amorphous silicon (a-Si:H) p-type crystalline silicon (c-Si) structures with and without a microcrystalline silicon (μ c-Si) buffer layer as a potential for hetero-junction (HJ) solar cell. Hydrogenated amorphous silicon and microcrystalline silicon film have been grown by inductively coupled plasma chemical vapour deposition (ICP-CVD). Solid phase crystallization (SPC) has been included to the process to improve the percentage of crystallization around 72%. The leakage current of HIT structure has been observed in the order of 10^{-8} Amp. It has also been indicated that the activation energy of the HIT structure is 0.795 eV at applied voltage is below 0.55 Volt.

Keywords—ICP-CVD process; Amorphous Silicon; Microcrystalline Silicon; Solid Phase Crystallization; Heterojunction

I. INTRODUCTION

We have used p-type 1-10 Ω cm <100>, crystalline silicon wafer for this study. The Si films were deposited in a planar coil ICP CVD reactor. In this system the intense degree of dissociation and ionization of silane is established in a region away from the substrate. Silane/helium mixture passes through a distribution ring located under the plasma region. Thus H₂ is directly dissociated while silane is dissociated predominately by active particles from the plasma region. The process pressure for PECVD and HDPCVD are quite different. More than 100 mTorr is common for PECVD. The pressure range of HDPCVD is 1~30 mTorr. We report on the study of 20 mTorr working pressure, 200~400°C substrate temperature, 200 Watt ICP power (13.56 MHz).

The high-density plasma was created by inductively coupling of RF energy to the plasma region through a silica plate. The silica plate was vacuum jointed to the top of the reactor. All other parts of deposition chamber were made from stainless steel. The ICP source diameter was about 20 cm. The samples were loaded on a grounded, resistance-heated stage. The planar coil to sample distance was 10cm. Aluminium metal was deposited on the back side of the crystalline silicon wafer using vacuum deposition technique. After rapid thermal annealing (RTA) microcrystalline silicon and hydrogenated amorphous silicon were deposited by inductively coupled plasma chemical vapour deposition technique. Around 10 nm thick Mg and 100 nm thick Al layer were deposited sequentially deposited and grid pattern was made by photo-lithography for the formation of top electrode.

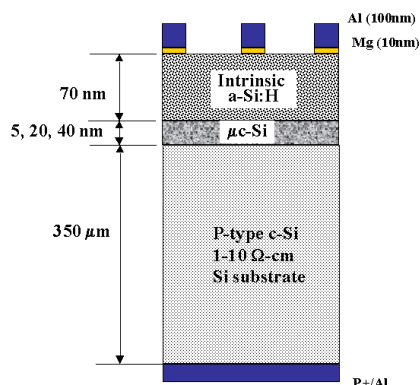


Fig.1 HIT cell structure

Fig.1 shows the schematic diagram of a typical HIT solar cell. We have used three different kinds of HIT cell structures for our present study. The first is one is the AL/Mg/ undoped a-Si:H/ undoped μ c-Si/ p-type C-Si/Al structure. The second type is AL/Mg/ undoped μ c-Si/ p-type C-Si/Al structure and the third type is the AL/Mg/ undoped a-Si:H/ p-type C-Si/Al structure. Current-voltage (I-V) characteristics of the solar cells were investigated using an Advantest R6243 calibrator under an illumination of 30mW/cm².

II. EXPERIMENTAL

We have used p-type 1-10 Ωcm <100>, crystalline silicon wafer for this study. The Si films were deposited in a planar coil ICP CVD reactor. In this system the intense degree of dissociation and ionization of silane is established in a region away from the substrate. Silane/helium mixture passes through a distribution ring located under the plasma region. Thus H_2 is directly dissociated while silane is dissociated predominately by active particles from the plasma

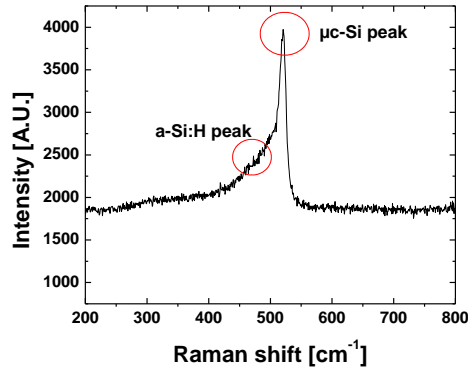


Fig.2 Raman Spectrum of $\mu\text{c-Si}$ / a-Si:H sample (a-Si:H 70nm and $\mu\text{c-Si}$ 20nm)

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III. RESULT AND DISCUSSION

The material properties of thin film silicon were critically analyzed with the help of Raman Spectrum. Fig.2. shows the Raman Spectrum of a-Si/ $\mu\text{c-Si}$ sample having thickness of a-Si was 70 nm and that of $\mu\text{c-Si}$ was 20 nm. Raman Shift peak of $\mu\text{c-Si}$ at 510 cm^{-1} and that of a-Si at 480 cm^{-1} were observed. Moreover from fig. 3,

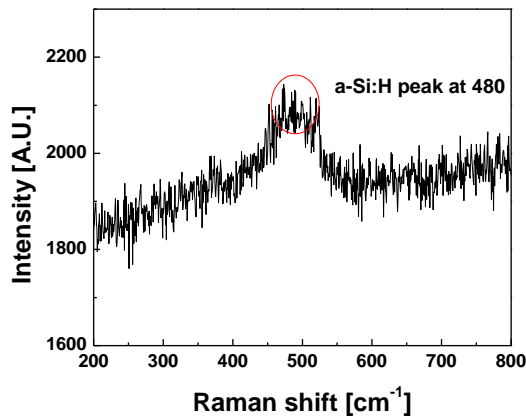


Fig.3 Raman Spectrum of $\mu\text{c-Si}$ / a-Si:H sample (a-Si:H 70nm and $\mu\text{c-Si}$ 5nm)

we have found that the Raman peak of $\mu\text{c-Si/a-Si}$ sample at 480cm^{-1} . In this experiment, we have used a-Si thickness 70nm and $\mu\text{c-Si}$ thickness 5nm respectively. Specially, film deposited at low temperature($\sim 250^\circ\text{C}$) followed by novel solid phase

crystallization(SPC) showed a crystalline peak at around 510cm^{-1} , showing that this film has a microcrystalline phase in an amorphous matrix.

Table-1: Crystallinity value of different samples

Substrate temperature($^{\circ}\text{C}$)	RF power in Watt	Crystallinity %
250	200	67
50	300	67
250	400	70
250	500	72

Table 1 shows the crystallized volume fraction of different experimental samples under different RF power for substrate temperature at 250°C . It was extracted from the equation $\gamma/[\gamma + 0.8(1-\gamma)]$, where γ is the fraction of the crystalline integrated intensity $I_c/(I_c+I_A)$. Here I_c represents the integrated intensity under the crystalline peak and I_A is the integrated contribution from the amorphous phase[12]. The maximum crystallization of 72% was achieved at RF power 500watt. High value of crystallinity helps to increase the photoconductivity value.

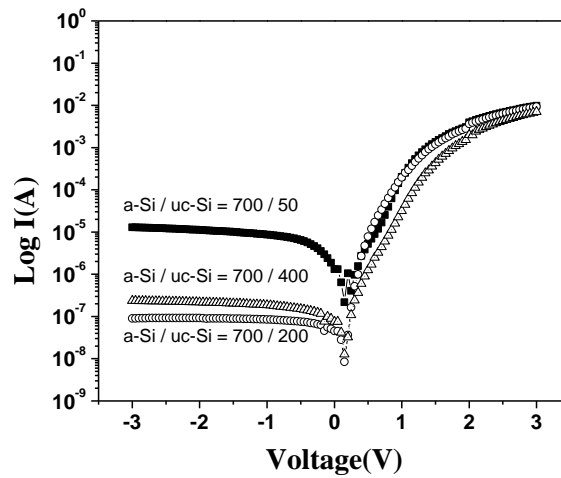


Fig.4 I-V Characteristic of a-Si:H / $\mu\text{c-Si}$ HIT Cell

Fig.4 shows the I-V characteristics of the a-Si/ $\mu\text{c-Si}$ HIT type cells. This cell with 20nm thick $\mu\text{c-Si}$ has a leakage current in order of 10^{-8} Amp. Fig.5 shows the J-V-T characteristics of the a-Si/ $\mu\text{c-Si}$ HIT having thickness 70nm of a-Si film and 5nm of $\mu\text{c-Si}$ film respectively. The expressions $J=J_0\exp(AV)$ and $J\propto\exp(-E_a/kT)$ were used for calculation of the activation energies of electron. Using Fig.6, the calculated activation energy was found 0.795eV.

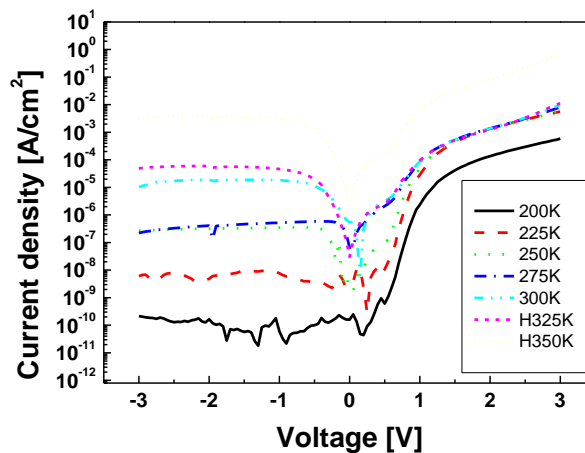


Fig.5 J-V-T Characteristic of a-Si:H / $\mu\text{c-Si}$ HIT cell at $V<0.5\text{V}$

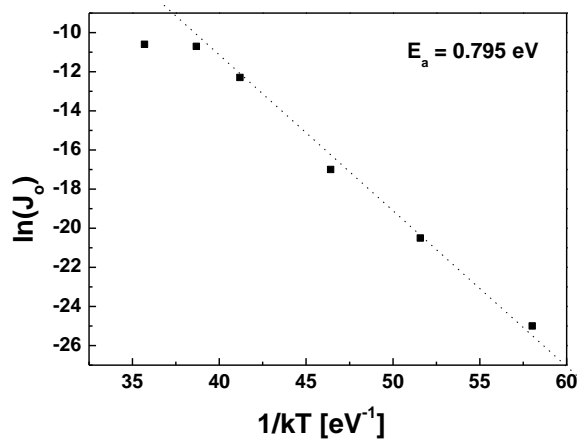


Fig.6 Temperature dependence of J_0 of the heterojunction when $0.3 < V < 0.50$

The J-V-T plots as shown in Fig.5 generally show a slope change at around $V=0.5V$, meaning that a different conduction mechanism start to dominate from this voltage until the conduction become spacecharge limited when $V>0.5V$. In addition, the relatively constant slope throughout this temperature range means that A is almost temperature independent as illustrated in Fig.5 for $0.3 < V < 0.5V$. This behavior is typical of the temperature independent conduction mechanism of tunnelling [13]. Among various tunneling mechanism, the conduction seems to follow the MTCE model, which is widely believed to be one of the dominant conduction mechanism in a-Si:H/c-Si heterojunctions. This is reasonably explained by both the increased probability of multistep tunnelling, resulting from the continuously distributed localized states within in the band gap of a-Si:H (or μc -Si) and the linear relationship between $\log J_0$ and $1/kT$ as shown in Fig. 6.

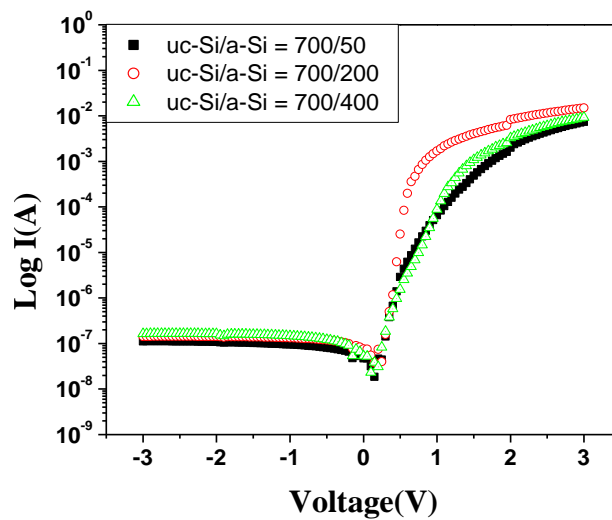


Fig.7 I-V Characteristic of a-Si:H of HIT cell

Fig.7 shows the I-V characteristics of a-Si HIT cell. From this figure the leakage current 50nm a-Si HIT was found as 2×10^{-7} Amp. Fig.8 shows the I-V characteristics of μc -Si /a-Si HIT. Type cell having 10^{-8} Amp. leakage current. This implies that the thickness of a-Si layer does not have any effect on the leakage current.

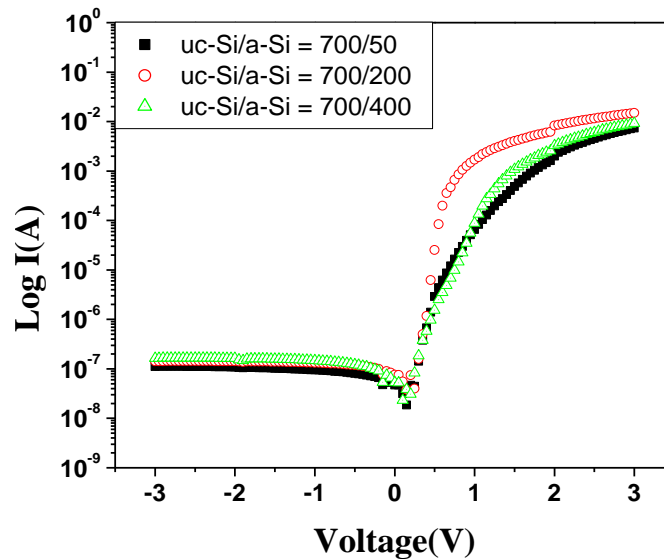


Fig.8 I-V Characteristic of $\mu\text{c-Si} / \text{a-Si:H}$ HIT cell

IV. CONCLUSION

In this paper, the feature of the HIT (heterojunction with Intrinsic thin layer) structure are reviewed. Around 72% crystallinity value of the $\mu\text{c-Si}$ film has been achieved using solid phase crystallization (SPC) method. The HIT Solar cell depicts a simple structure and a low processing temperature (250°C). The leakage current is in the order of 10^{-8} Amp. in I-V Characteristic of the HIT type cells. Hit cell activation energy is determined as 0.795eV when the applied voltage is below 0.5V .

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