

Failure Mechanisms in Ceramic Capacitors

Multilayer ceramic capacitors (MLCs) have become one of the most widely used components in the manufacture of surface mount assemblies, and are inherently very reliable. However, all ceramics are brittle, and when layout design and manufacturing methods do not take this into account, these normally trustworthy devices can fail unexpectedly, either immediately or (arguably much more seriously) during service.

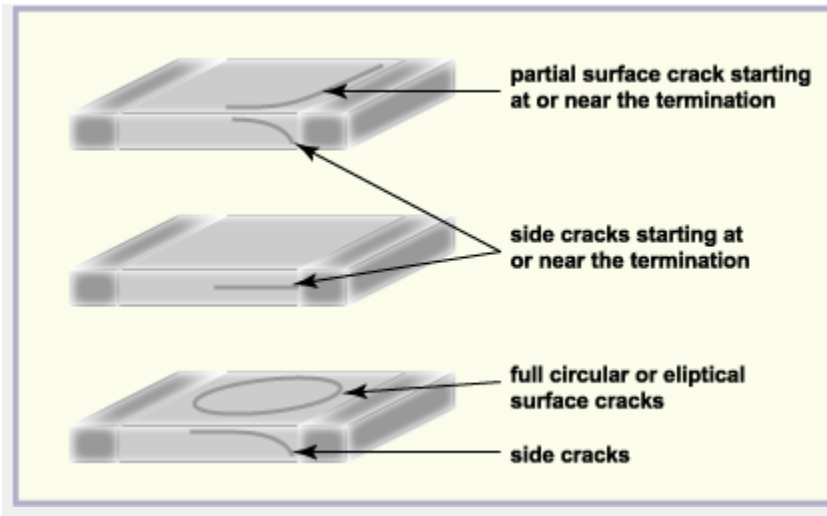
Design and process issues

One cause of unreliability is failing to design boards to minimise the considerable thermal stresses to which MLCs are subjected during soldering. These arise from mismatches in CTE, both between the capacitor and the board on which it is mounted and between the different materials which make up the capacitor.

The MLC is constructed of alternate layers of silver/palladium (Ag/Pd) alloy, with a CTE of around 20 ppm/°C, and ceramic with a CTE of 10–12 ppm/°C. When this composite structure is heated, the electrodes tend to force the capacitor apart. This tendency is made worse by Ag/Pd being a much better conductor of heat (>400 W/m.K) than ceramic (4–5 W/m.K), so that a thermal gradient will exist across the ceramic layer.

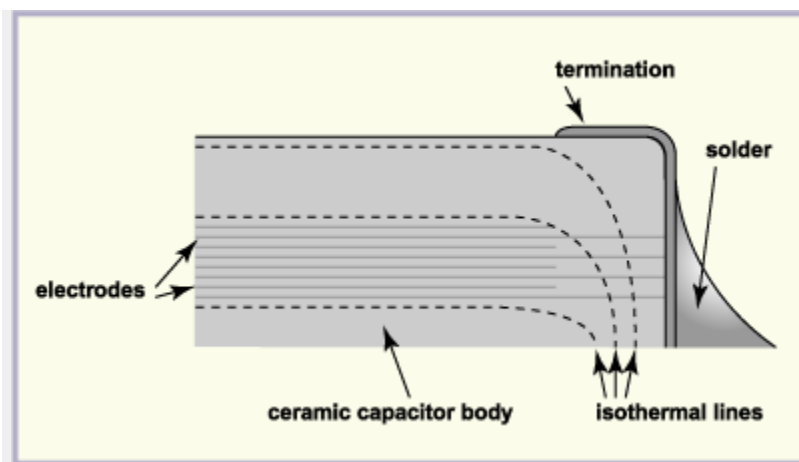
The solder terminations also expand at a greater rate (25–30 ppm/°C) than the ceramic part and exert an annular tensile force on the edges of the component. In severe cases, when a large surface mounted capacitor has been subjected to a sudden thermal shock, a clearly visible elliptical crack may form on the upper surface of the chip (Figure 1). This is primarily due to the tensile forces exerted by the terminations.

Figure 1: Extreme thermal shock cracks in MLCs



Less obvious is the creation of micro-cracks under the visible surface of the capacitor, which propagate along isothermal lines within the component (Figure 2). This form of damage is particularly insidious, since electrical failure may not occur until some time after assembly, when the finished product is out in the field.

Figure 2: Micro-cracking under thermal stress



After a number of temperature excursions, for example due to circuit operation, the crack may propagate (Figure 3), creating an open-circuit device. In severe cases, the body of the capacitor may even fall out, leaving just remnants of ceramic surrounded by termination and solder joints.

Capacitor missing after severe cracking

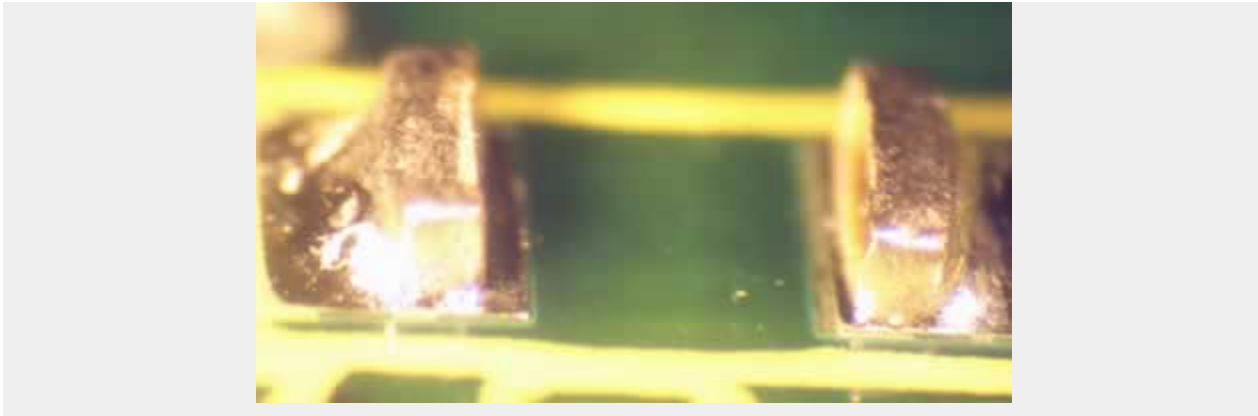
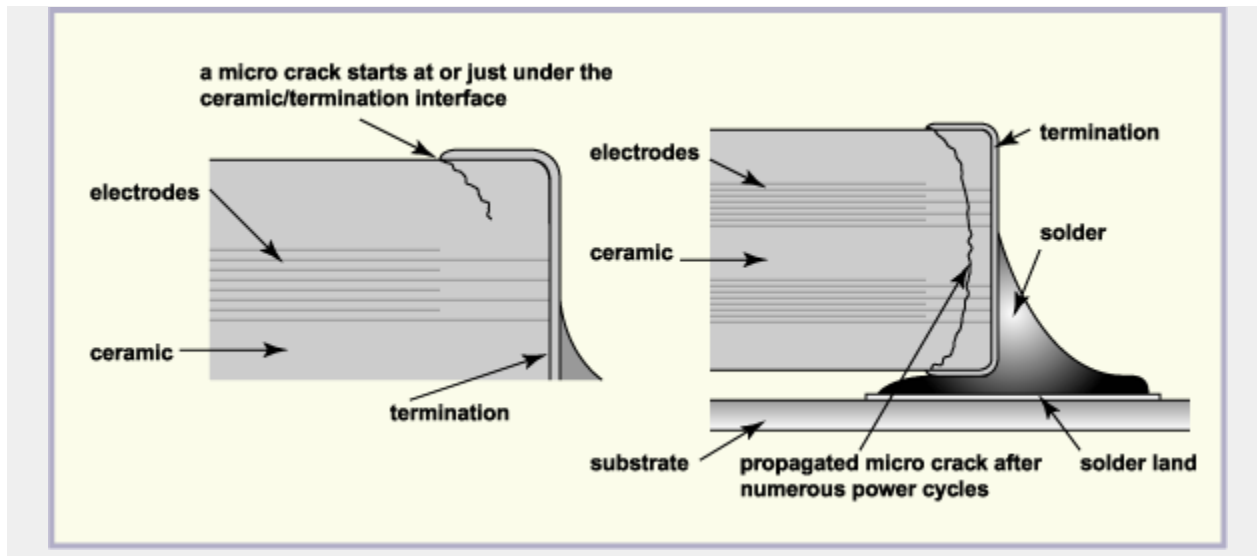


Figure 3: Propagation of a micro-crack



Fortunately, improvements in ceramic technology have reduced the incidence of both types of crack, at least as far as well-made components are concerned. It has been commented that the reflow process is unlikely to cause failures unless parts have already been damaged.

However, component reliability can be further improved by appropriate choice of soldering conditions:

- Most problems in wave soldering can be overcome by reducing the solder bath temperature (to 235–245°C) and controlling the pre-heat

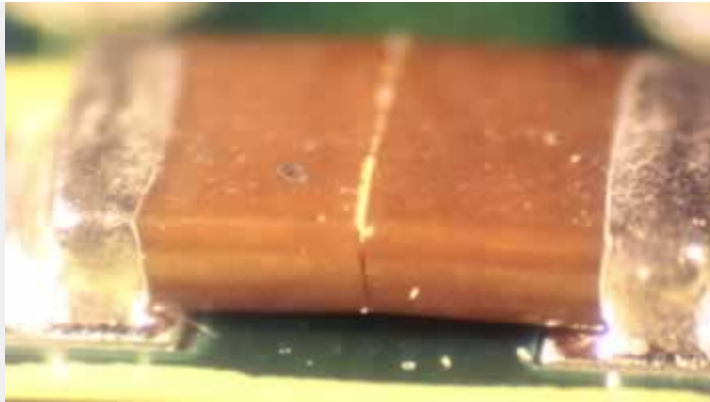
- In reflow soldering, excessively high rates of temperature rise during preheat should be avoided, as these can cause micro-cracking. The conditions for minimum failure rates depend on the reflow process used, but it is usually recommended that MLCs should not be subjected to rates of change of temperature of more than 2°C/second. There is some evidence that a steady rate of change is more important than the absolute rate of heating, and that the rate of cooling is less important than the rate of heating
- Hand soldering during rework has been shown to damage components, so it is recommended that the iron bit should never come into direct contact with parts, instead using solder for heat transfer.

Although most components are now correctly specified and manufactured for surface mounting, this was not always the case, and reference should always be made to the manufacturer's data sheets. Where a simple thermal shock test is needed, this can be done by immersing sample parts in a solder bath at 260°C (simulating the worst case soldering process), testing the parts electrically both before and after solder immersion.

Handling damage

When a circuit board is bent, its shape tries to become an arc of a circle, as far as the rigidity of the attached components will allow. The outer surface stretches and the distance between the component lands is increased, placing the chip under tension: conversely, on the inner surface, an MLC is exposed to compressive strain. Whilst any joint will stress-relieve, given time, in the short term only a limited degree of stress reduction can come from deformation of the solder joint. If the forces applied to the chip exceed its breaking strength, the chip will crack!

Cracked capacitor

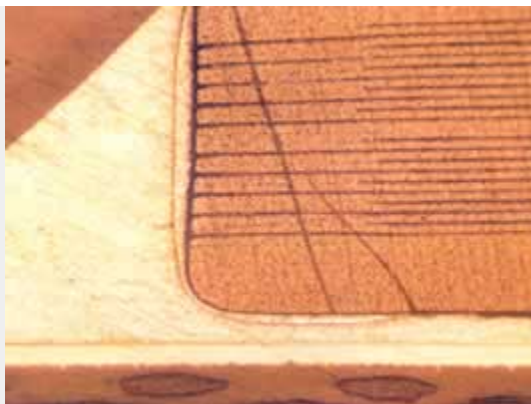


Stress is a force which produces (or tends to produce) deformation, and is measured as the force applied per unit of area.

Strain is the deformation which results from a stress, and is measured as the ratio of the change to the total value of the dimension in which the change occurred. As with CTE, strain is dimensionless, and usually quoted in 'micro-strain'.

Figures for the maximum level of strain which can be tolerated by an MLC vary between suppliers and between types, but may be as low as 1000–1500 micro-strain.

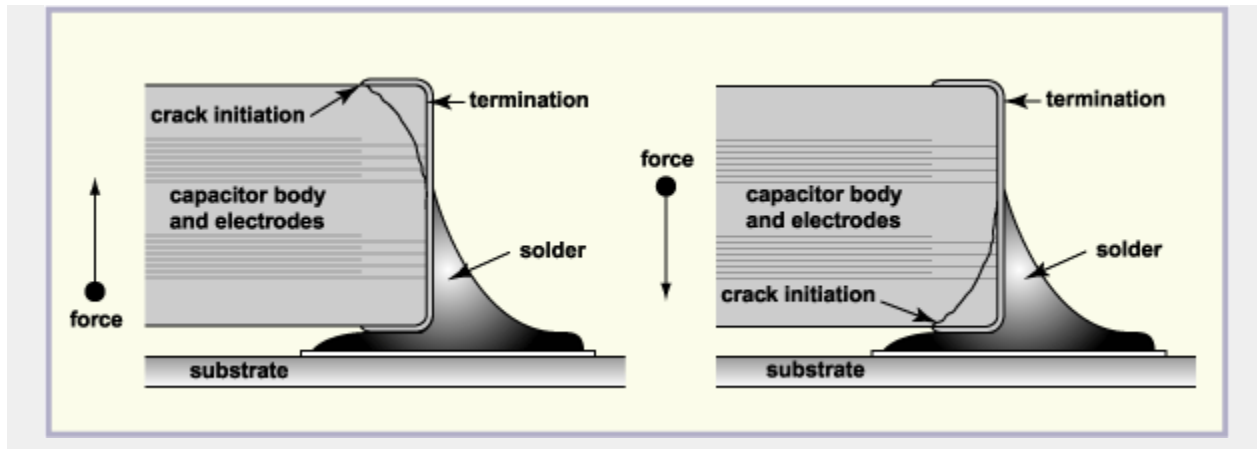
Bending-induced cracks in an MLC



Cracks which are created as a result of board bending typically look quite different from thermally-induced cracks, being contained within the terminated

area, as shown in Figure 4, running from the edge of the termination towards the end face of the chip.

Figure 4: MLC cracking due to board stress or warpage



The consequences of these cracks are serious, especially as they are usually not visible, and immediate changes in key parameters are rare. Syfer Technology report that 'cracks are visible at the exterior in less than 2% of affected parts and change of capacitance is a feature of no more than about 10% of broken chips'. The parameter affected is usually insulation resistance (IR), where some 60% of damaged parts exhibit a detectable change. However, only a small minority are actually identified as potential failures before use. The problem is complicated in a number of ways:

- In-circuit tests can rarely apply sufficient voltage and/or time for realistic IR measurement
- The electrical problem may be intermittent, with the failure masked during manufacture as a result of thermal treatment or by probe pressure, but failing later
- Most functional tests are not sensitive even to the omission of capacitors used in common decoupling or EMC suppression applications

- Similarly, many decoupling or EMC suppression capacitors may be damaged and defective without affecting circuit function in normal conditions.

Most seriously, what starts as a modest reduction in IR can degrade to the point where the circuit fails to work, due to penetration of the crack structure by atmospheric moisture. Total short-circuits are less common, but have been known to cause catastrophic board loss (from burn-out) in designs where the fault current was not limited.

The presence of micro-cracks can in theory be detected by subjecting the chip to a high voltage insulation resistance test at 85°C and 85% relative humidity. However, several other factors may also lower the insulation resistance in this way, especially poor choice of cleaning solvents, or the use of solvents containing large amounts of dissolved flux residue.

More sensitive tests for micro-cracks and delamination apply a mobile ionic material such as methanol to the part, measuring IR changes. However, the effects can be similarly obscured by contamination.

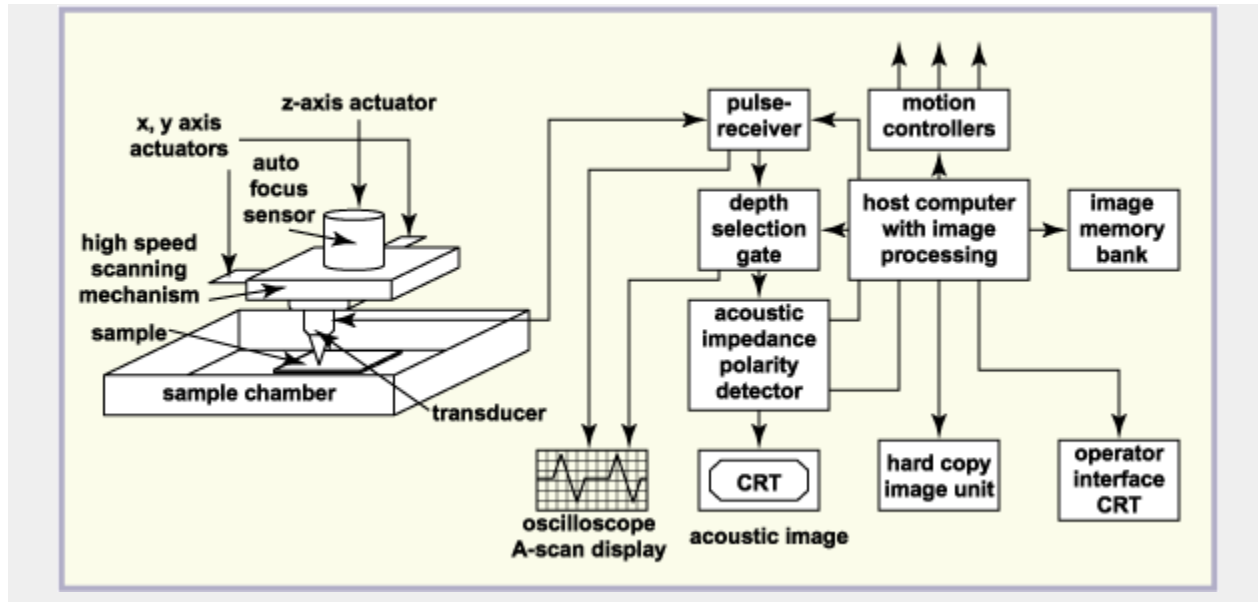
An alternative (and non-destructive) method is scanning acoustic microscopy (SAM), which uses an ultrasonic transducer, typically operating at 10MHz to 100MHz, with the component immersed in fluid (usually water) to couple it to the transducer. The ultrasound travels through the material until it reaches interfaces or discontinuities, which reflect some of the energy.

SAM systems operate in three modes:

- **reflection mode**, where sound reflected from the sample gives a high resolution image of the surface and near surface
- **transmission mode**, which creates contrast between areas of different density and signal attenuation, looking at the whole thickness of the sample
- **C mode** (Figure 5), designed for moderate penetration, where ultrasonic energy is focused at an appropriate plane within the

sample, and the phase of the reflected wave indicates the density of the material through which it has passed.

Figure 5: Schematic of C-SAM principle



SAM can produce direct images of defects within a sample, such as discontinuities, voids and inclusions. The technique has a broader range of application than X ray radiography, because it is not limited to materials of high atomic weight.

Causes of flexure damage

There are many source of potential damage to components caused by board flexure, most of which are listed below:

- Board support pins used for second side printing (or placement) making direct metallic contact with parts on the underside
- Insufficient board support during second side placement, leading to excessive board flexure

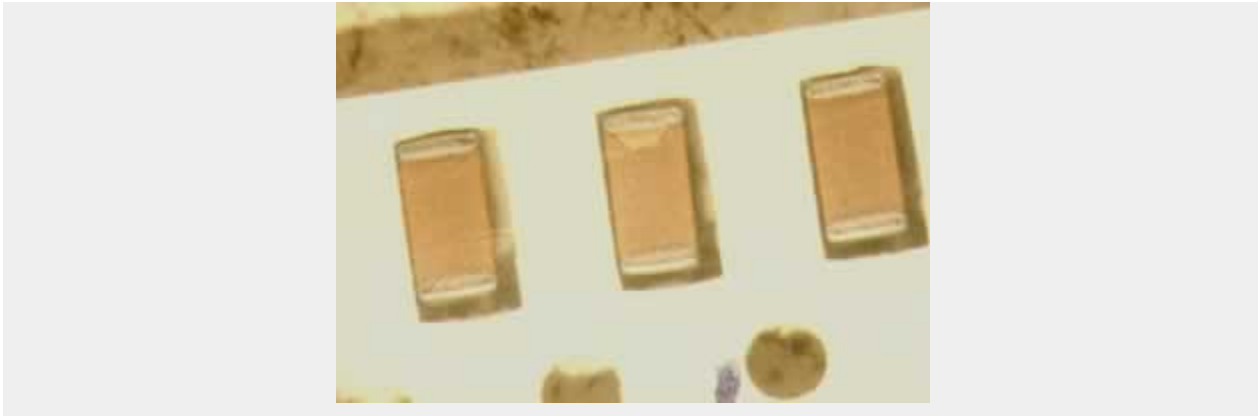
- Incorrect height of board support pins, or over-clamping, leading to the board being bowed upwards during second side placement or printing
- Damaged placement nozzles
- Over-pressure and/or nozzle over-travel during placement cycle: few placement machines have any direct control of the actual placement pressure
- Board sag during wave or reflow soldering, caused by poor support, followed by a subsequent straightening process (such as printing, in-circuit test or box build)
- Boards becoming caught in conveyors
- Separation of individual circuits from master panels ('break-out' or 'de-panelling')
- Careless operator board handling, especially when pressing a board into retaining clips, connectors, or boxes

Capacitor cracking due to placement damage



When investigating cracking problems, it must be remembered that cracking may occur at an early stage, but only be exposed by the mechanical and temperature stresses of a later assembly process. In the past, components have even been found to be damaged before removal from their packaging!

Capacitor cracked before mounting

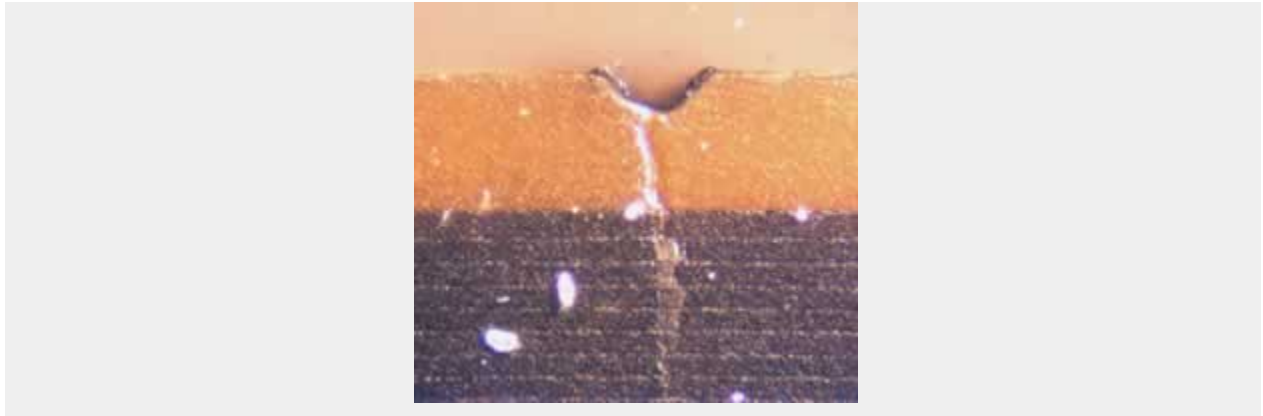


It should also be borne in mind that board flexure may take place in use, due to shock and vibration. The extent of any problem will depend on the operational environment and on the degree of support offered by the next layer of assembly. In particular, the design of the structure should be examined to make sure that there are no opportunities for board resonance: board flexures and their associated stresses can be very much higher than normal when an assembly is excited at its resonant frequency.

Expect the unexpected

When you investigate failures, you should always expect the unexpected. Chip ceramic capacitors are usually unmarked, because of the practical problems of doing this. However, some end customers, particularly in the automotive industry, prefer capacitors to be marked, so that they can have visual assurance that the correct component has been fitted. Given the small dimensions of the components, the most obvious method for marking is to use a laser to 'write' on the ceramic surface. Provided that this is carried out with appropriate power levels, this coding is effective and not damaging. However, if too high a power setting is chosen, then the laser coding can generate cracking down into the sensitive dielectric area. As we explained earlier, cracks are always bad news!

Capacitor damage due to excessive laser marking



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